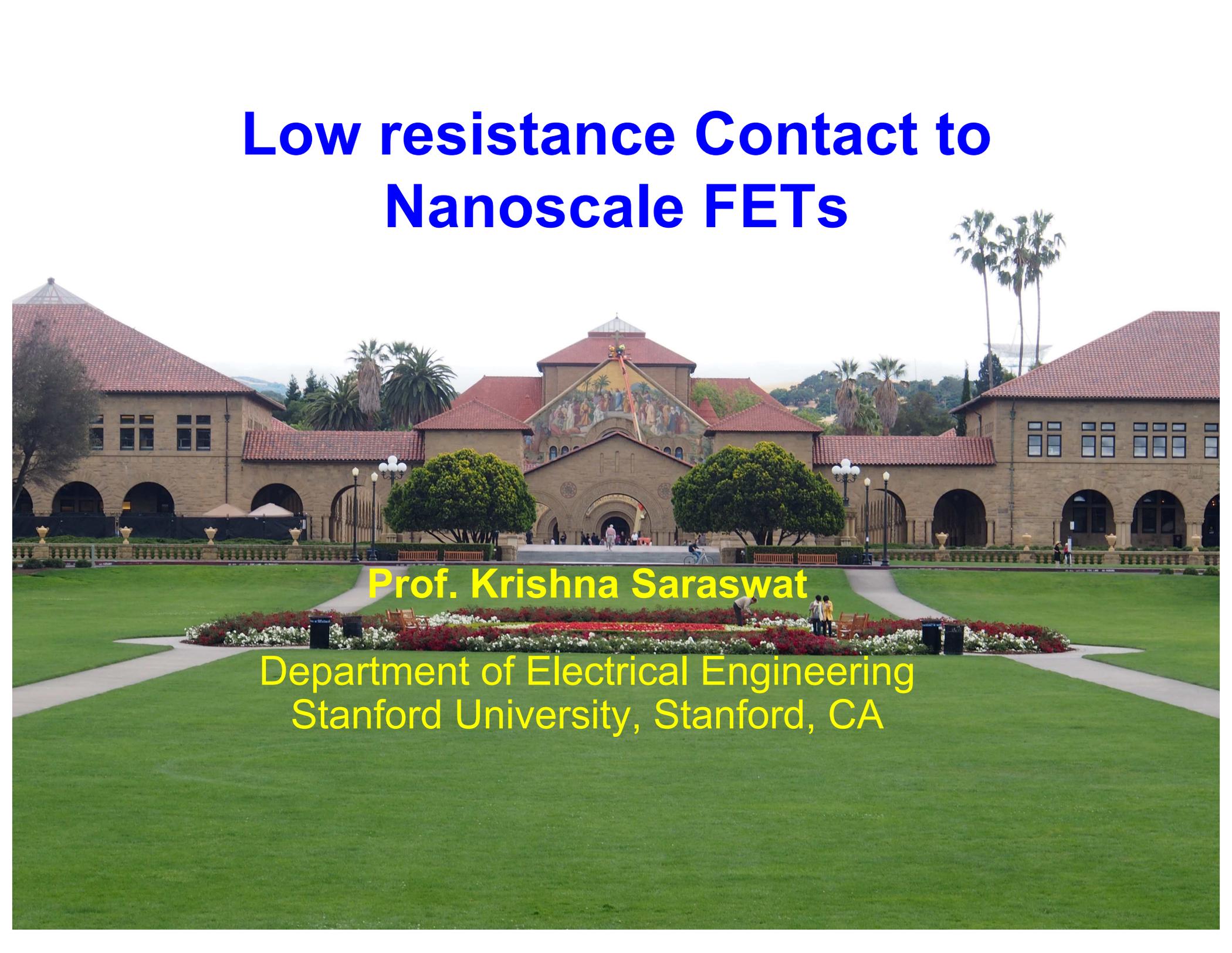


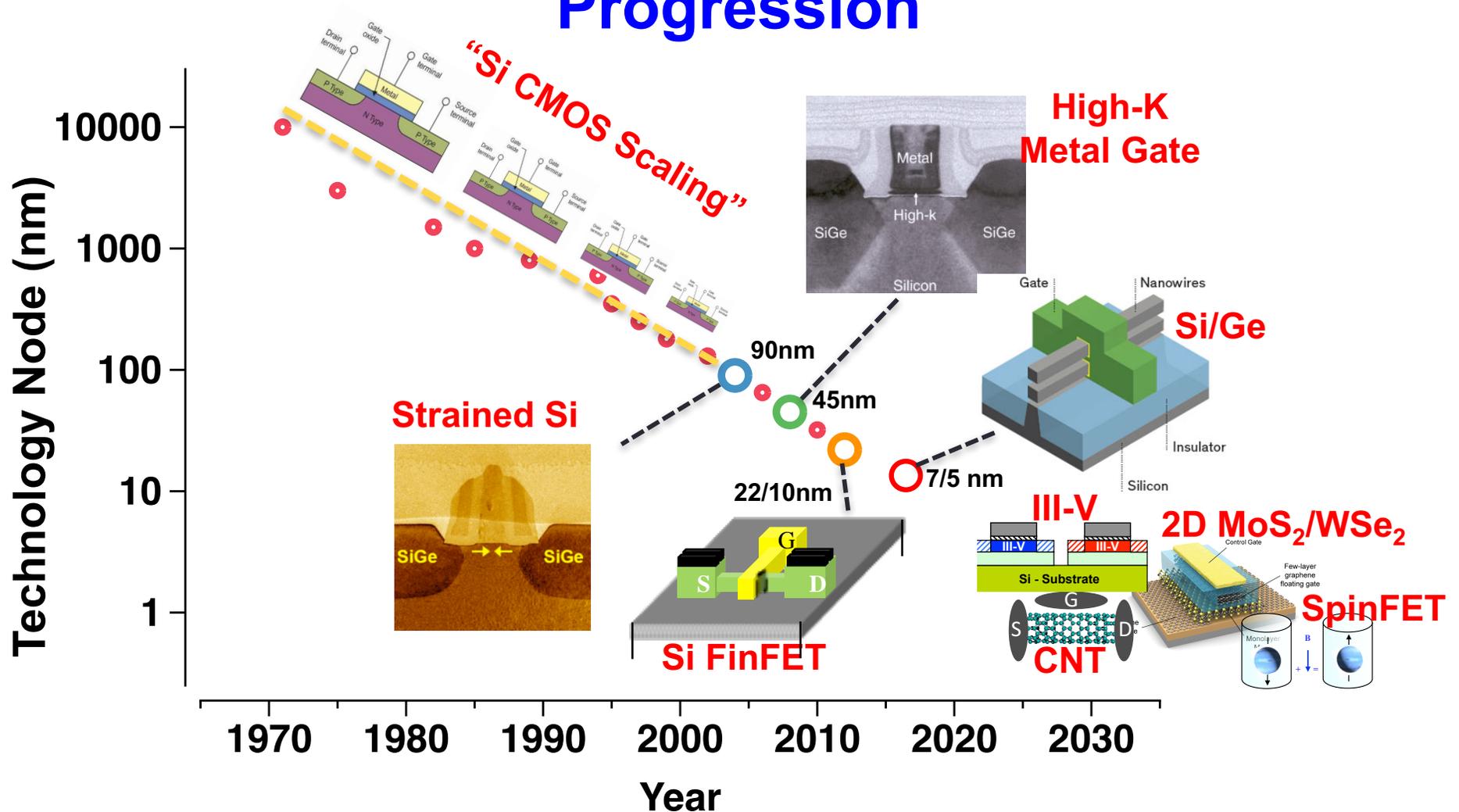
Low resistance Contact to Nanoscale FETs

A wide-angle photograph of the Stanford University Main Quad. The central focus is the red-tiled, sandstone building with a large mural above the entrance. The foreground is a large green lawn with a central flower bed and two paths leading towards the building. Several people are visible walking on the paths and near the flower bed. The sky is overcast.

Prof. Krishna Saraswat

Department of Electrical Engineering
Stanford University, Stanford, CA

New Materials/Structures for MOSFET Technology Progression

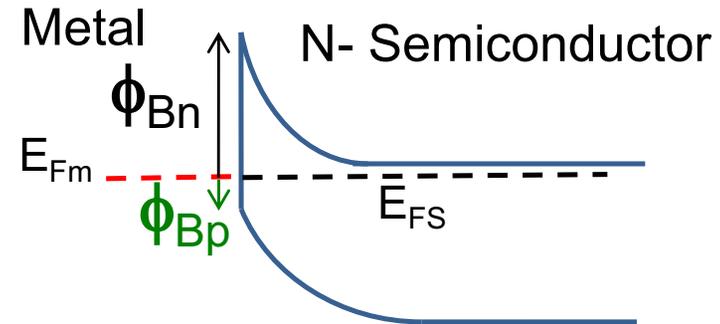
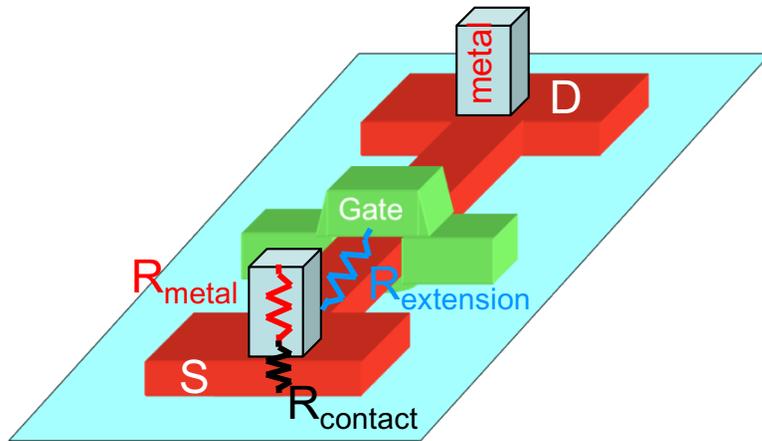


- Moore's law in the past relied on shrinking Si MOSFETs
- Moore's law in future demands more than just shrinking transistors
 - New materials and device structures **integrated on Si**

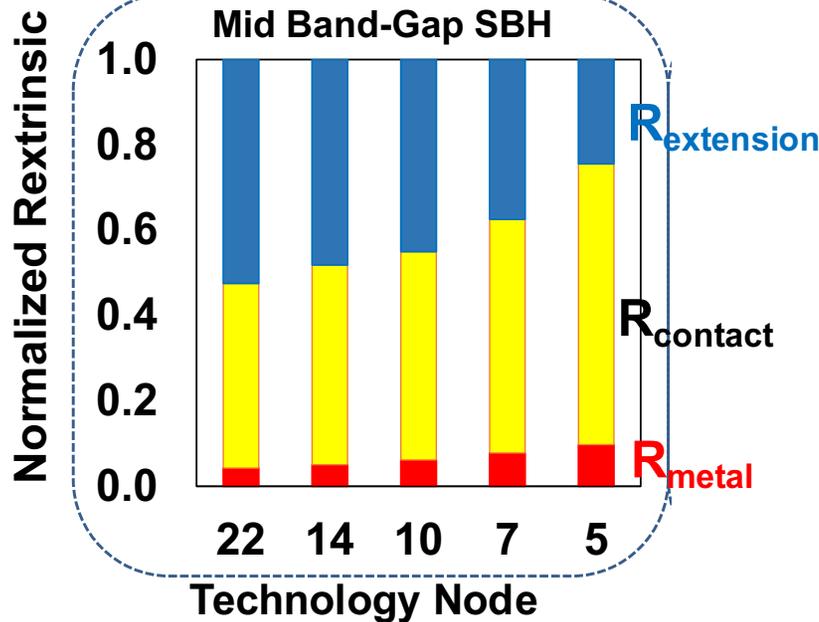
What is the Problem?

- To go beyond limits of Si higher performance material like Ge, III-Vs (?), carbon nanotubes and 2D materials like MoS₂ provide a promising path to continue Moore's law
- However, as device scaling continues, parasitic source resistance largely dominated by contact resistance, is beginning to limit the device performance

Contact Resistance



$$I_{DS}^{SAT} = \left[(V_{GS} - V_T) - I_{DS} R_{SD} \right]^2$$

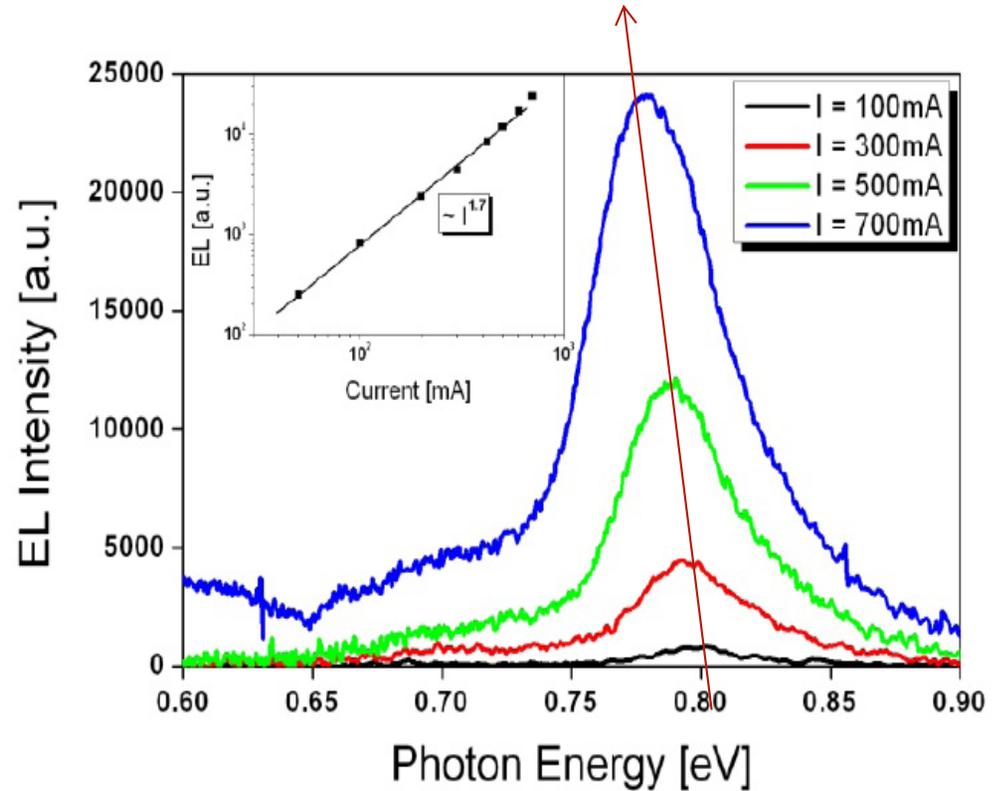
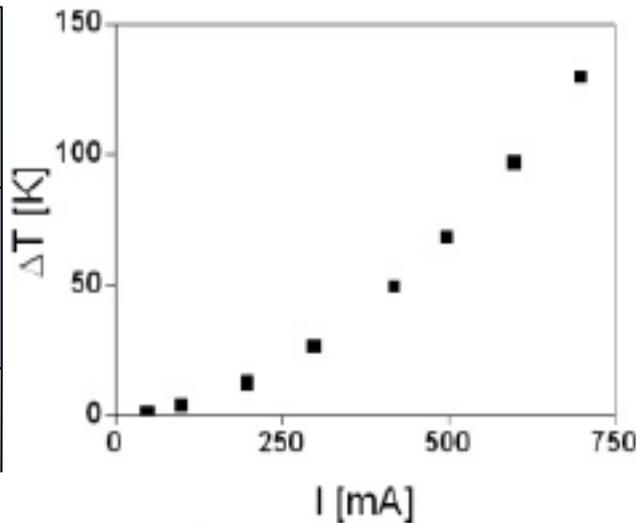
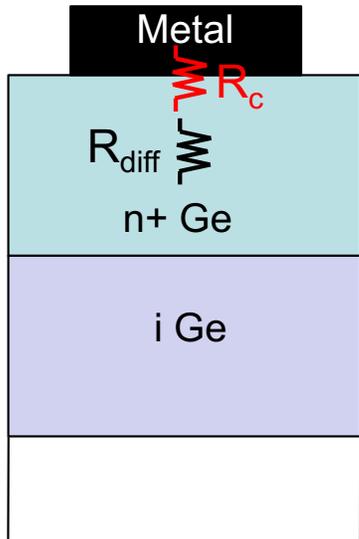
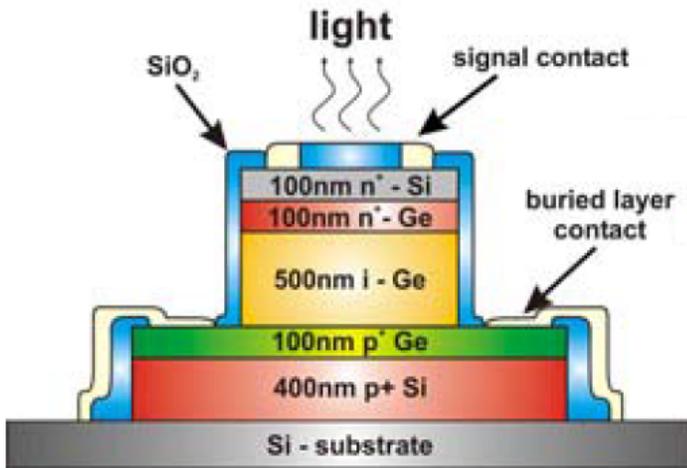


$$\rho_c = \rho_{co} \exp\left(\frac{2\phi_B}{q\hbar} \sqrt{\frac{\epsilon_s m^*}{N}}\right) \text{ ohm-cm}^2$$

- Contact resistance $R_c \propto \rho_c / A_c$
- Contact area A_c goes down with scaling
- Active doping N limited by solid solubility
- Barrier height ϕ_B needs to be reduced

S. Datta, et al., VLSI Symp, 2014

Contact Resistance Problem: Photonics



- Direct band gap emission from Ge p-i-n heterojunction photodiode.
- Shift in wavelength with higher current density
- Power dissipation through $R_c + R_{diff}$ heats the diode
- Need contacts with $\rho_c \sim 10^{-9}$ ohm.cm² for future electronics and photonics

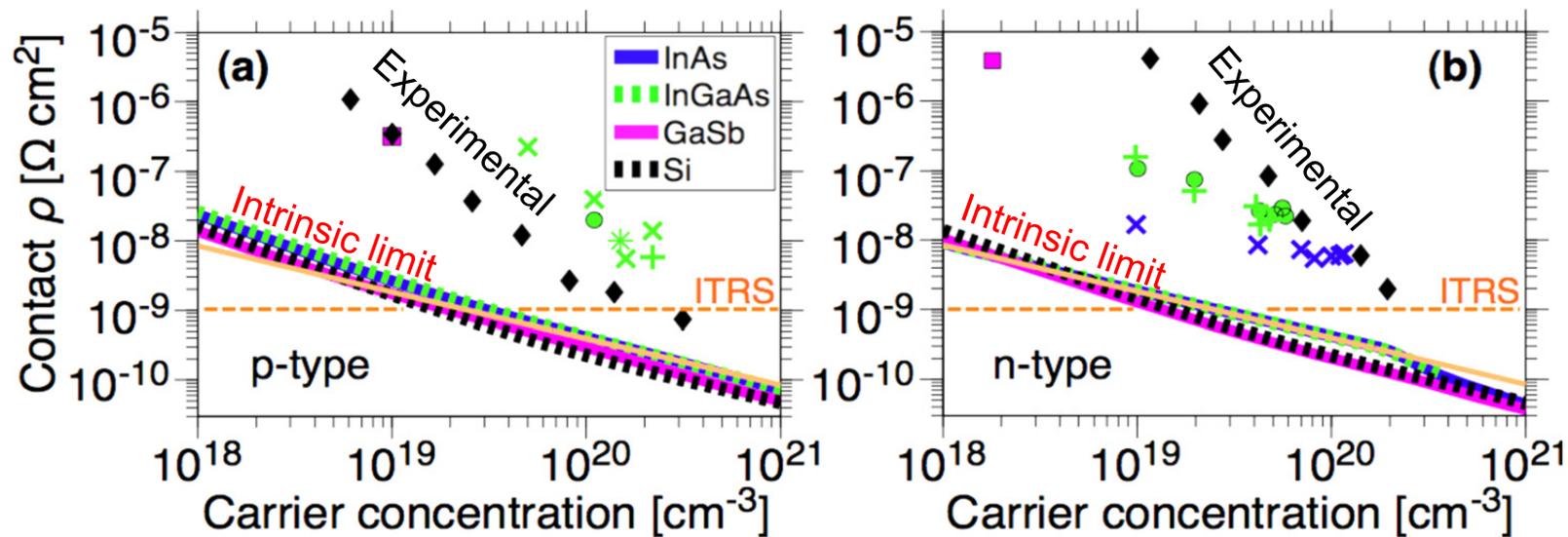
Conductance Quantum: Landaur Limit

- **Conductance quantum** in ideal 1D wire with M propagating modes and T transmission probability

$$G = (2q^2/h)MT$$

- Using this approach the intrinsic lower limit of **contact resistivity** is:

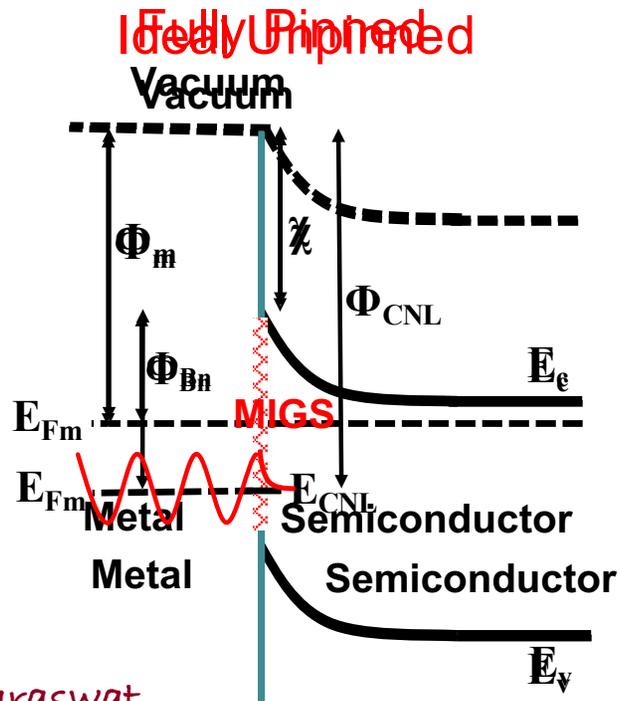
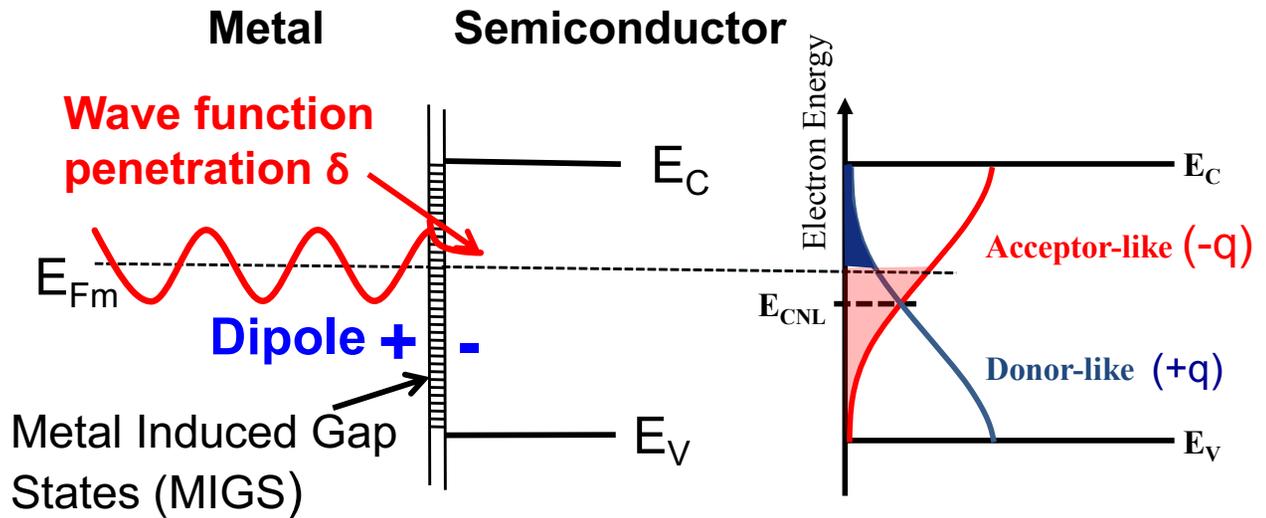
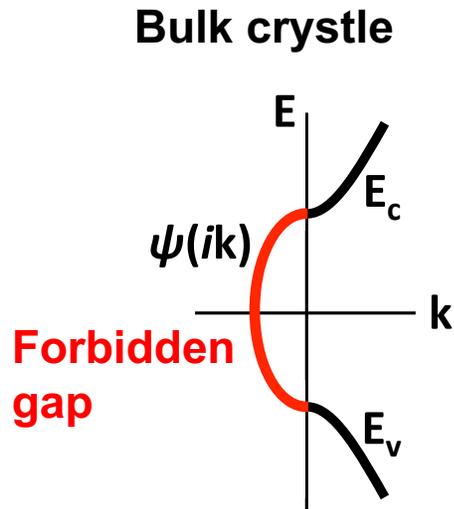
$$\frac{1}{\rho_c^{LL}} = \frac{4q^2}{h} \int_{-\infty}^{+\infty} M(\epsilon) \left[-\frac{\partial f}{\partial \epsilon} \right] d\epsilon, \quad [\Omega^{-1} \text{m}^{-2}]$$



- Assumptions in QM modeling
 - Ideal metal with enough conducting channels (very large M)
 - Realistic band structure of semiconductors (limited M)
 - Ballistic transport between metal and semiconductor - no scattering
 - **Zero Schottky barrier, no Fermi level pinning**, transmission coefficient $T = 1$

Need zero M/S barrier and heavy doping to lower ρ_c

Fermi Level Pinning \rightarrow Fixes ϕ_B



MIGS density $D_{IS} = 2/(\pi a^2 E_g)$

Unpinned barrier height $\phi_{Bn} = \phi_m - \chi$

Pinned barrier height

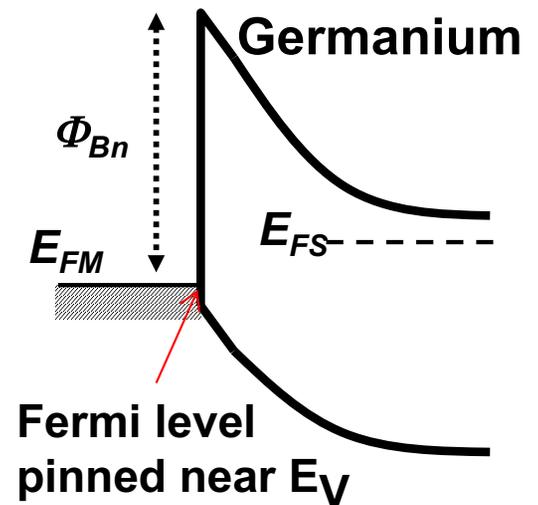
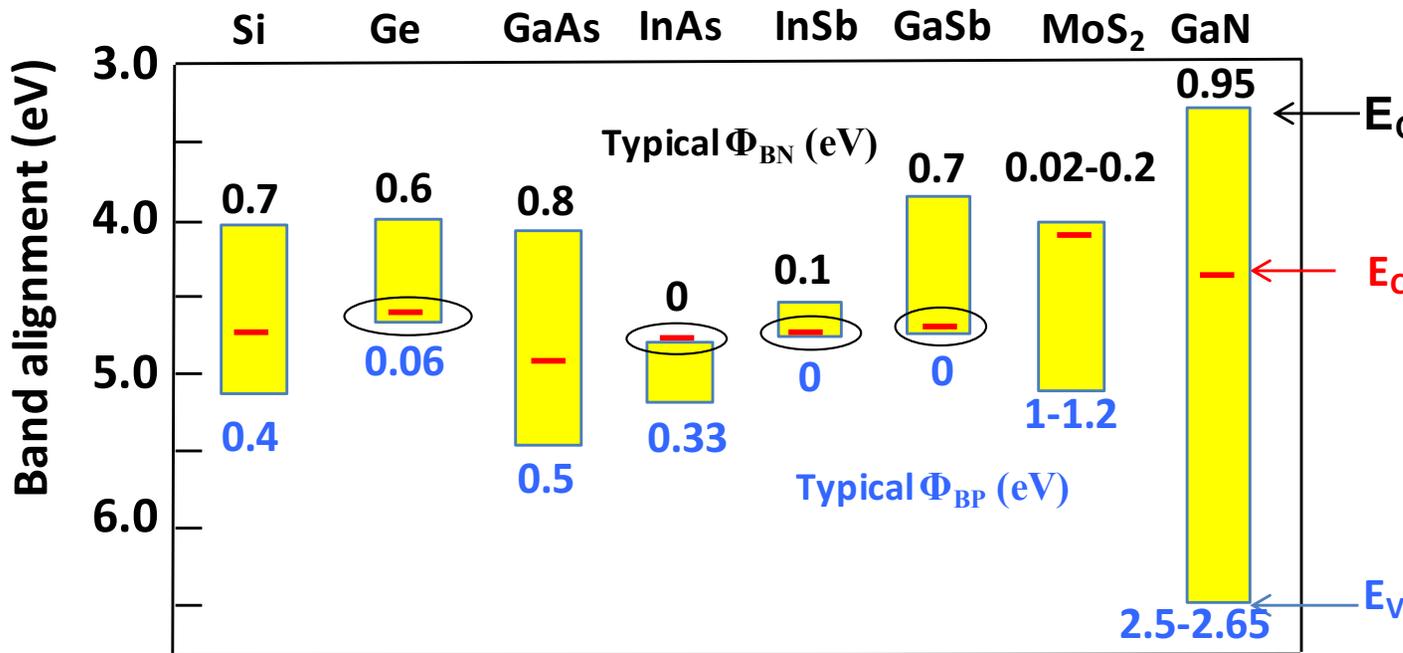
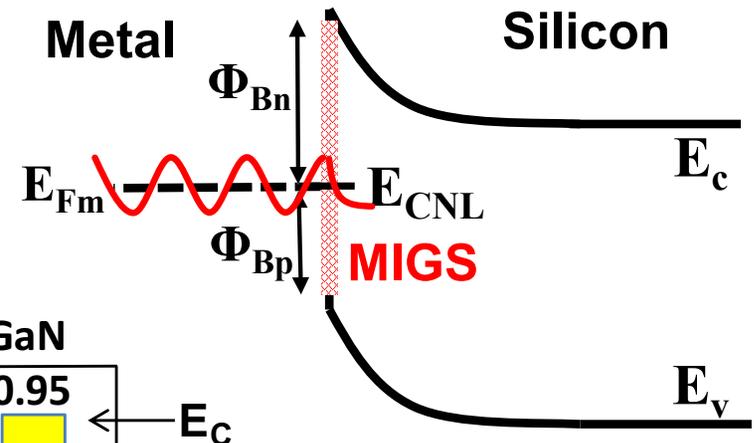
$\phi_{Bn} = S(\phi_m - \phi_{CNL}) + (\phi_{CNL} - \chi)$

Pinning factor $S = \frac{d\phi_{Bn}}{d\phi_m} = \left[1 + \frac{D_{is} e^2 \delta}{\epsilon} \right]^{-1}$

W. Monch, Phys. Rev. Lett., **58**,1260, March 1987.

Fermi Level Pinning → Fixes Barrier Height ϕ_B

- Metal wave function penetration
- Metal induced gap states (MIGS)
- Fermi level pins near E_{CNL}

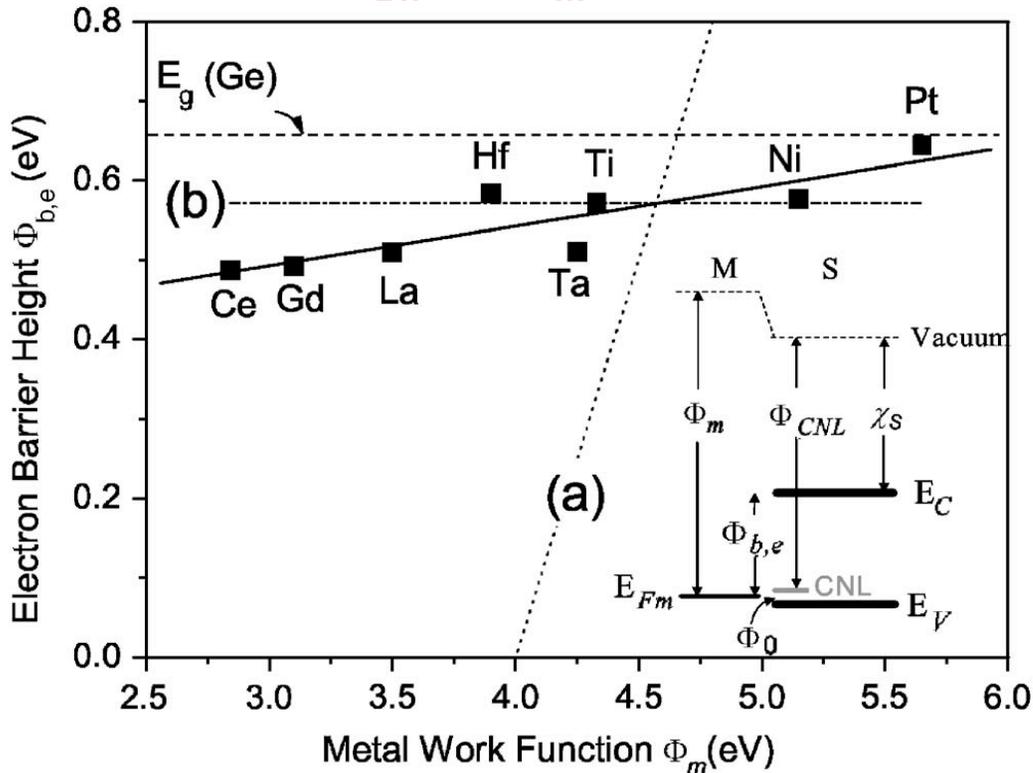


Fermi level pinned near E_v
 $\Phi_{Bp} \approx 0$ and
 $\Phi_{Bn} \approx E_g$

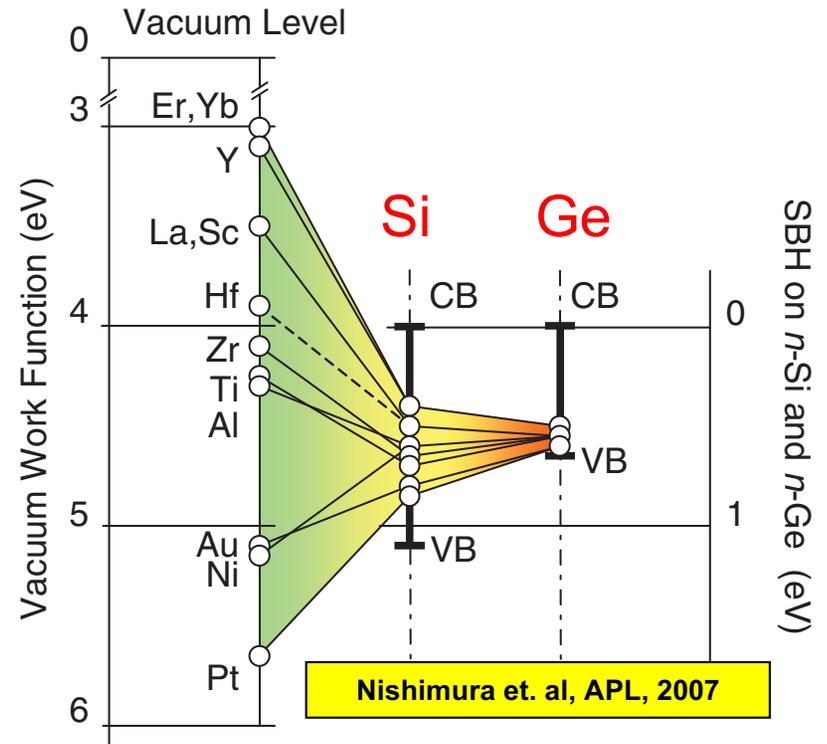
- Most semiconductors have strong pinning
- Excellent ohmic contacts to p-Ge, n-InAs, p-InSb
- Poor contacts to n-Ge, p-InAs, n-InSb, n-GaSb.

Pinned Schottky Barrier Height

Φ_{Bn} vs. Φ_m for Ge



Dimoulas, APL 89, 252110 (2006)



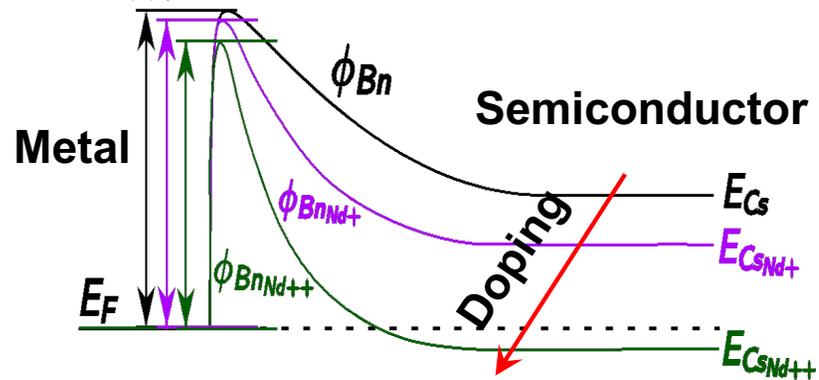
Nishimura et. al, APL, 2007

$$\text{Ge } \Phi_{Bp} \approx 0 \text{ and } \Phi_{Bn} \approx E_g$$

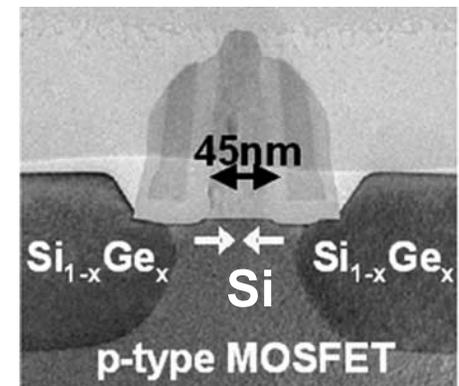
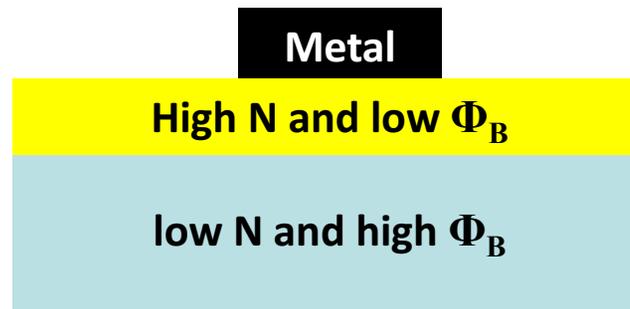
$$\text{Si } \Phi_{Bp} \approx E_g / 3 \text{ and } \Phi_{Bn} \approx 2E_g / 3$$

Approaches for Low Resistance Contacts

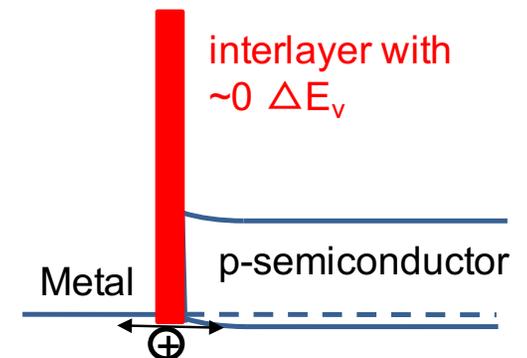
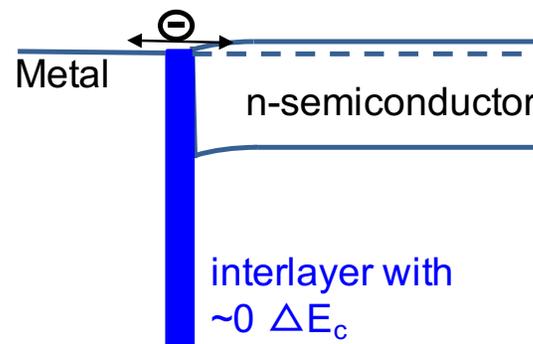
Decrease barrier thickness by increasing doping.
Best for n-Si, p-Ge, n-InAs



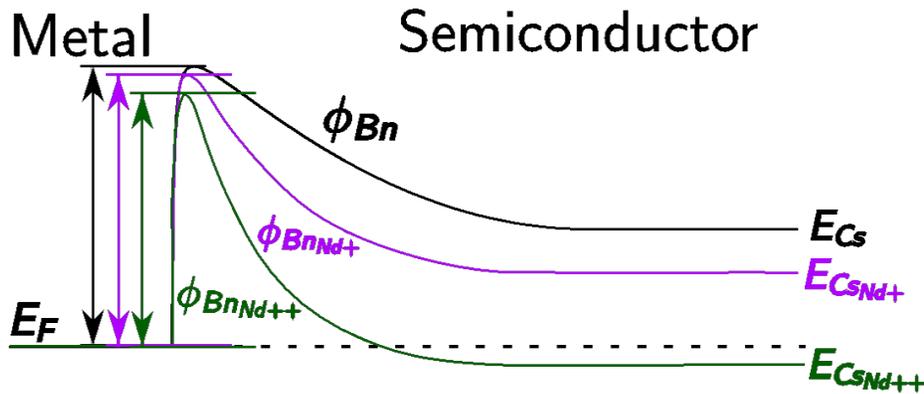
Heterostructures
 e.g., p-Ge on p-Si
 n-InGaAs on n-Ge



De-pinning Fermi level by metal - interlayer - semiconductor (MIS)
ZnO, ITO for n-contacts
NiO for p-contacts



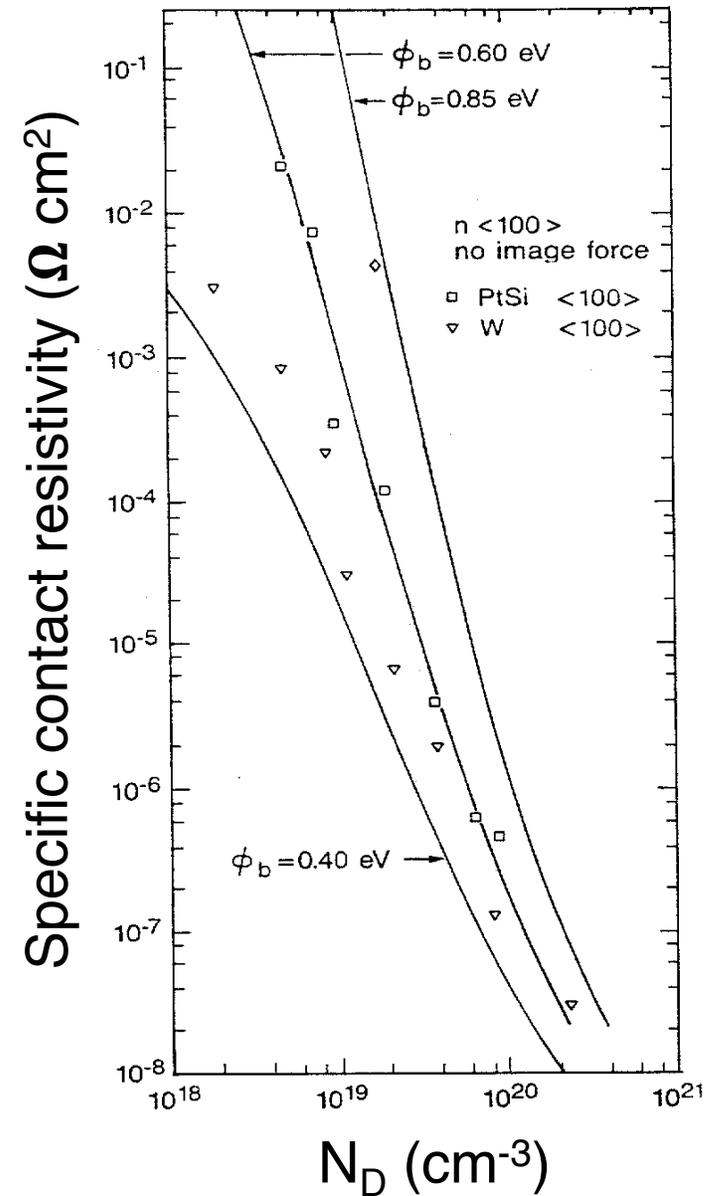
Specific Contact Resistivity of MS Contacts to Si



$$\rho_c = \rho_{co} \exp\left(\frac{2\phi_B}{q\hbar} \sqrt{\frac{\epsilon_s m^*}{N}}\right) \text{ ohm-cm}^2$$

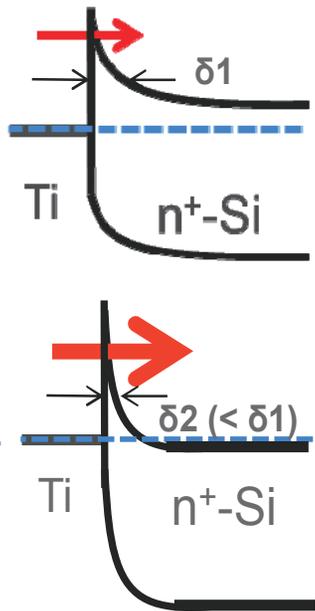
Specific contact resistivity ↓

- As doping density ↑
- Barrier height ↓
- Need to reduce barrier height ϕ_B and increase active dopant density N



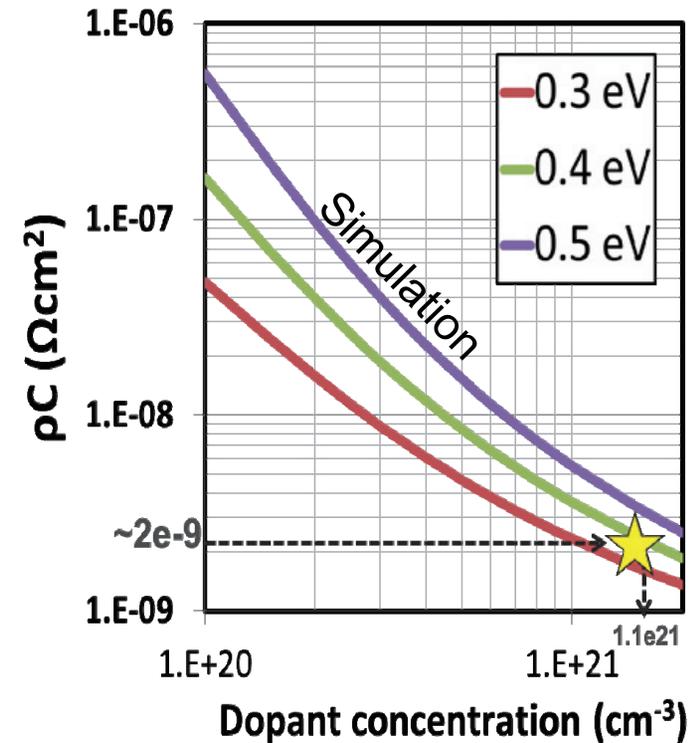
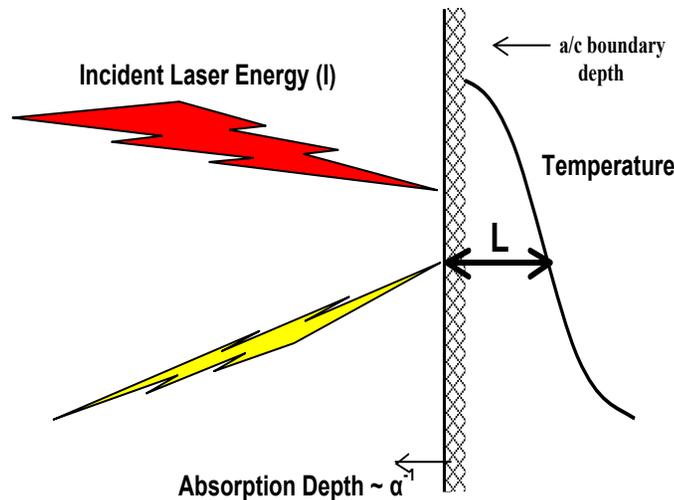
S. Swirhun, Electrochem. Soc. 1988

Low ρ_c by heavy doping in contacts to n-Si



- Heavy doping
- Reduced barrier
- Higher tunneling

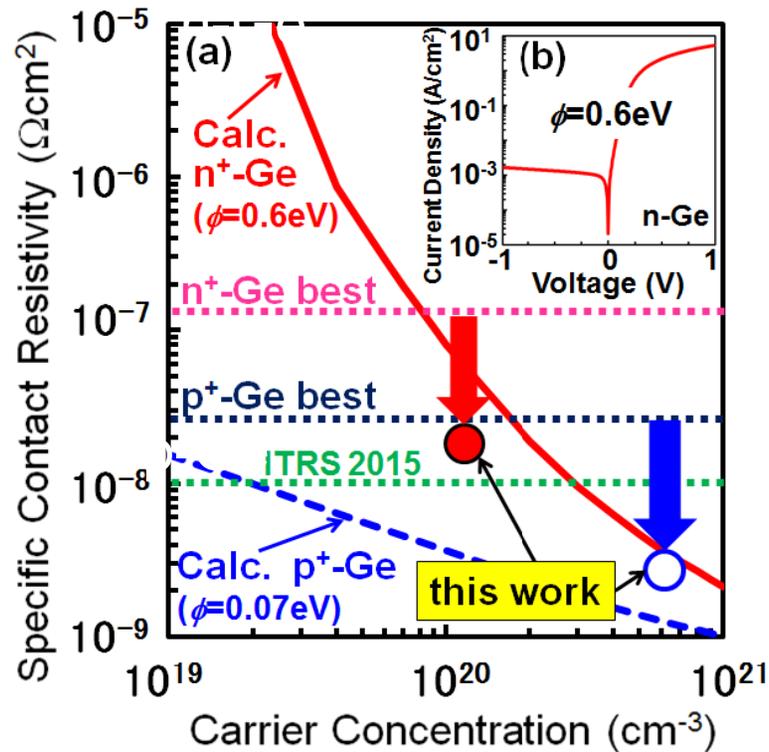
laser anneal activation



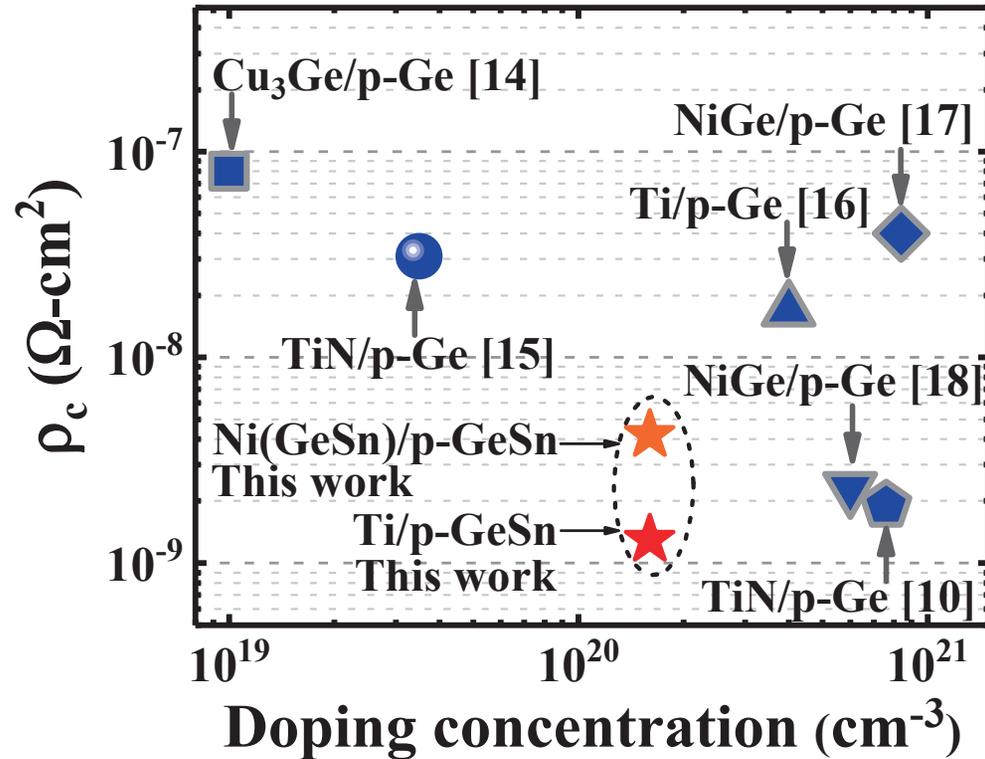
C.-N. Ni, et al., 2015 Symposium on VLSI Technology

- Conventional doping methods give $\rho_c \sim 10^{-8}$ ohm.cm²
- It is possible to get *metastable* electrically active doping density higher than the equilibrium doping density $> 10^{21}$ cm⁻³
- Low contact resistivity has been demonstrated in n-Si
- **Thermal stability of laser annealing is problematic?**

Low ρ_c by heavy doping in contacts to p-Ge/GeSn



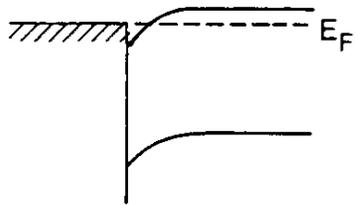
H. Miyoshi, et al., 2014 Symp. VLSI Tech.



Y. Wu, et al., 2017 Symp. VLSI Tech.

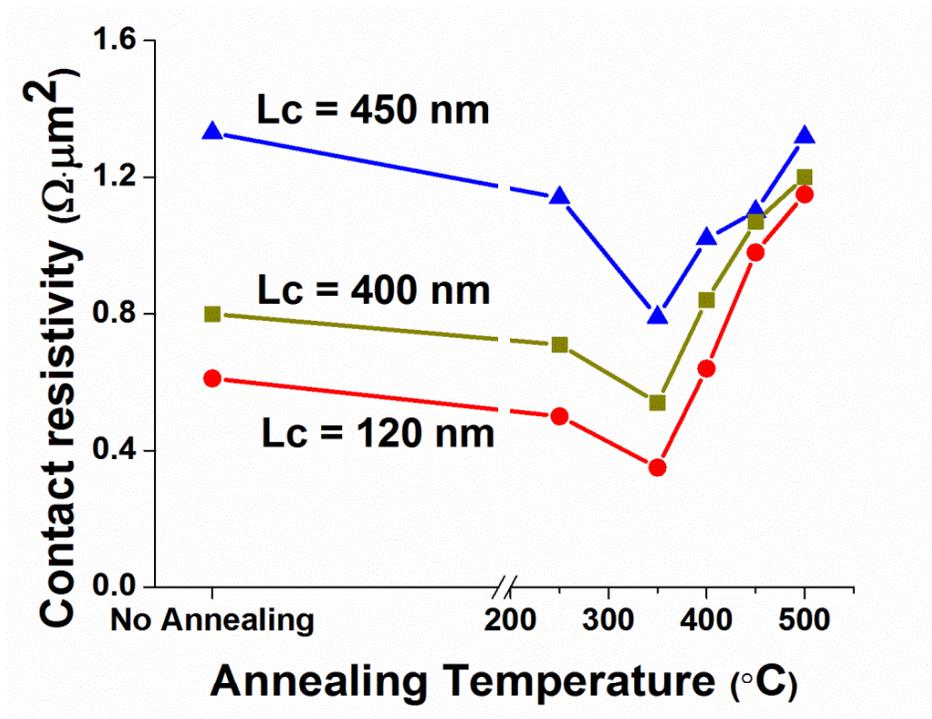
- p-Ge: $\rho_c = 2 \times 10^{-9} \Omega\text{cm}^2$
- p-GeSn: $\rho_c = 1.2 \times 10^{-9} \Omega\text{cm}^2$ with Ga doping
- N-Ge: Laser anneal enhances $n = 1.9 \times 10^{20} \text{cm}^{-3}$ and $\rho_c = 1.9 \times 10^{-8} \Omega\text{cm}^2$
 - ρ_c to n-Ge still higher than to p-Ge

Contacts to III-V NMOS (InGaAs)

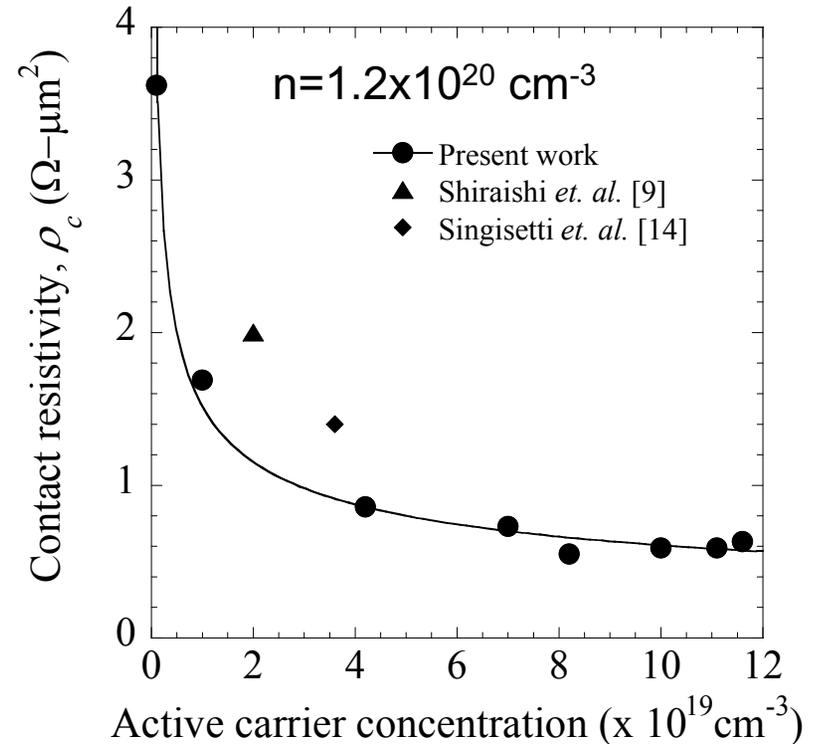


- Fermi level pins in the conduction band $\rightarrow \Phi_{BN} \sim 0$
- With moderate doping it is possible to get low ρ_c

Mo/InGaAs



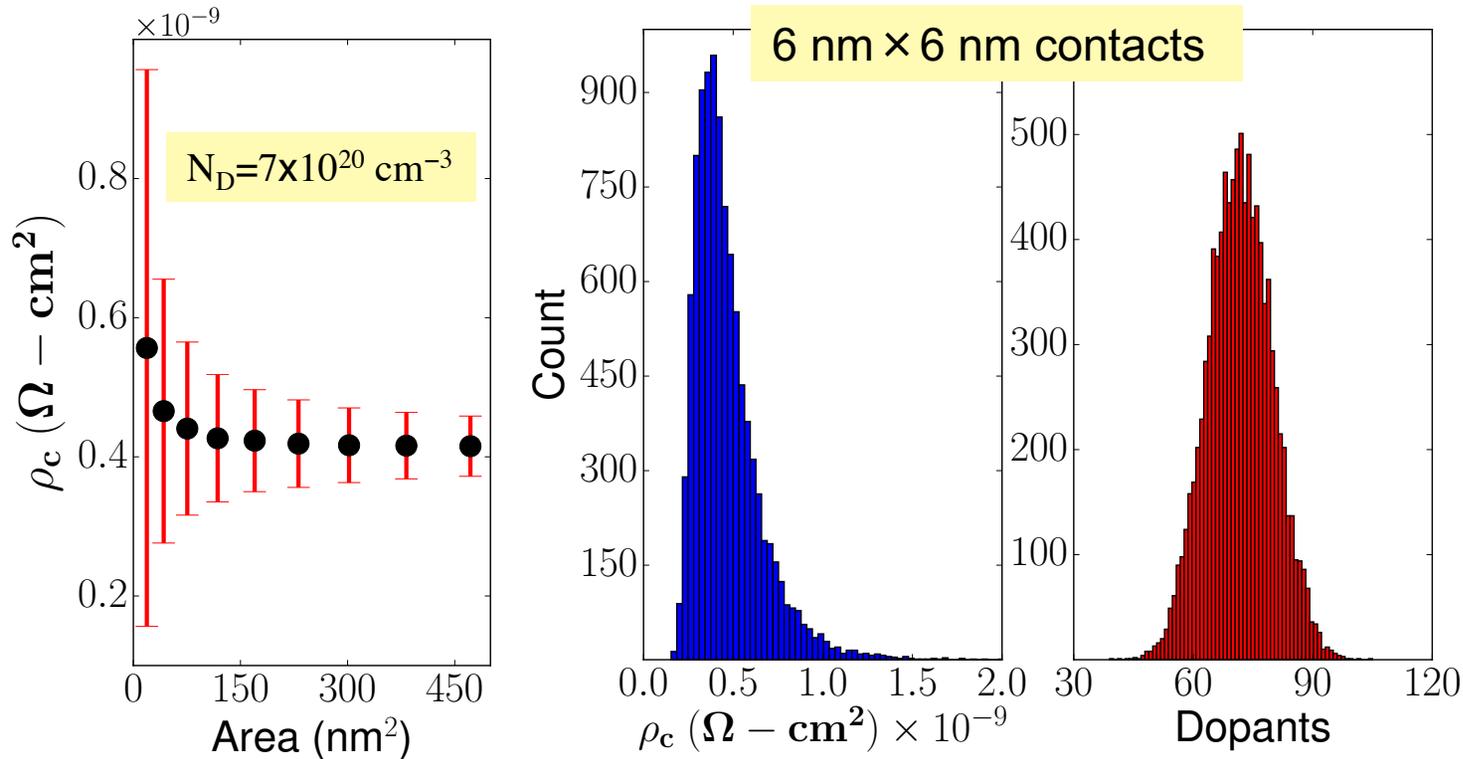
$$\rho_c = \sim 6.7 \times 10^{-8} \text{ ohm-cm}^2$$



$$\rho_c (\text{min}) \sim 5 \times 10^{-9} \text{ ohm-cm}^2$$

A. Baraskar, et al., 2010 IPRM

Statistical Variation in Nanoscale Contacts in Si

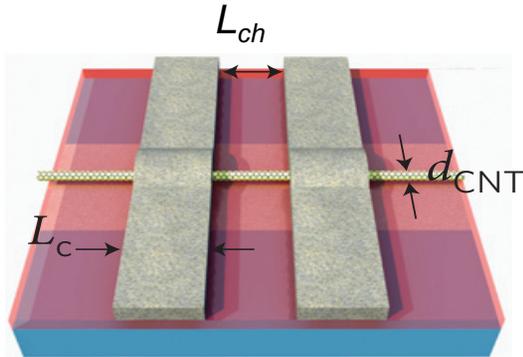


- Si with $N_D = 7 \times 10^{20} \text{ cm}^{-3}$
- Contact resistivity shows increasing mean and variance as dimensions decrease
- The empirical distribution of ρ_c in 6 nm \times 6 nm contacts shows high variance and skew.

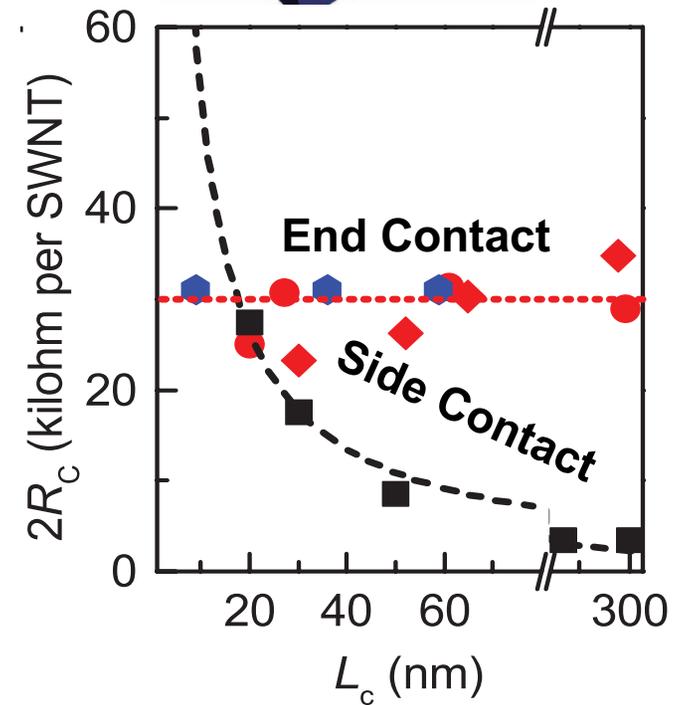
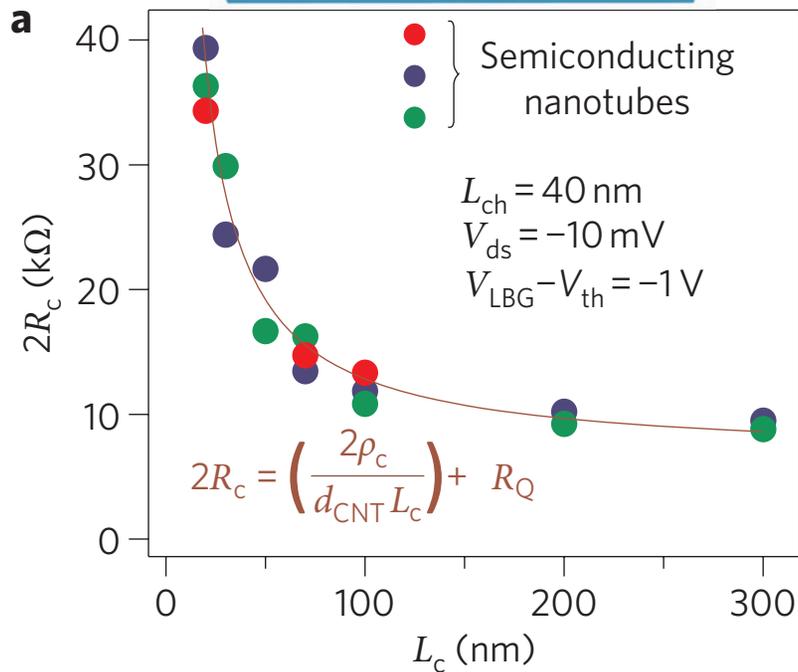
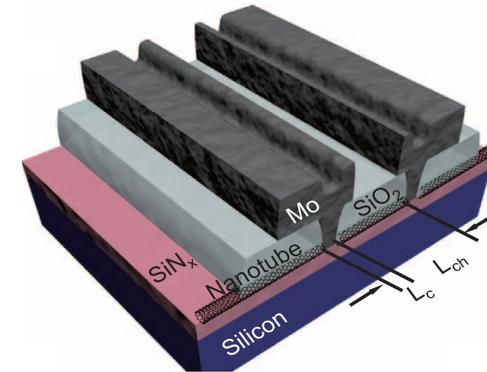
G. Shine & K. Saraswat, IEEE TED, Sept. 2017.

Contacts to Carbon Nanotubes

Top contact



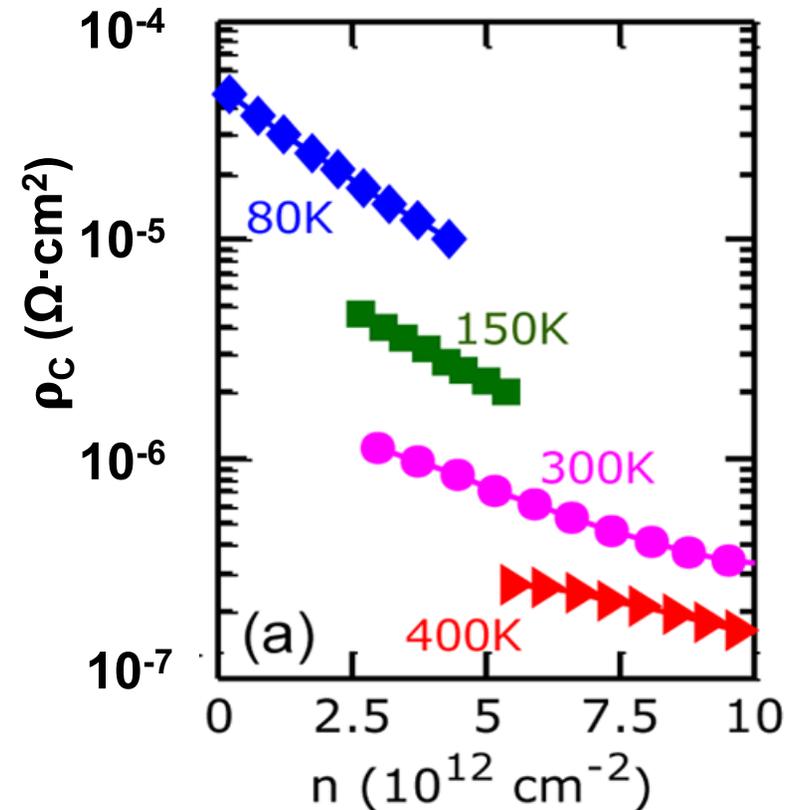
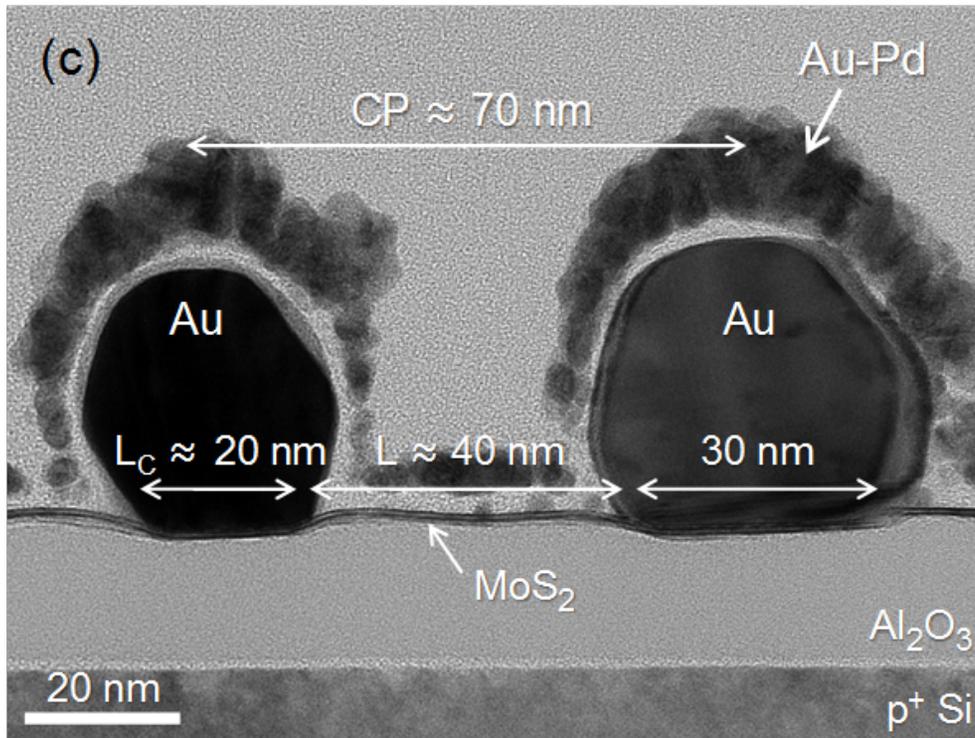
Side contact



Franklin and Chen, Nature Nanotech. Dec. 2010

Qing Cao, et al., Science, Oct. 2015

Contacts to MoS₂



- **Smallest MoS₂ contacts to date**

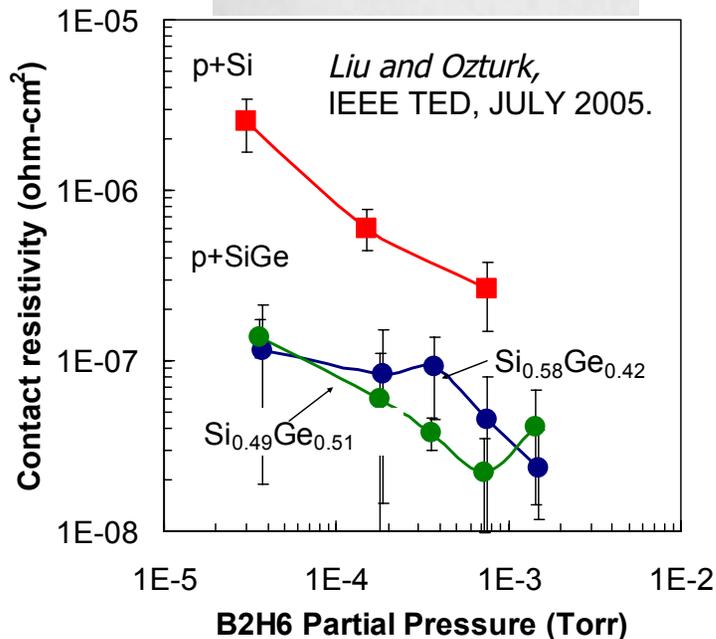
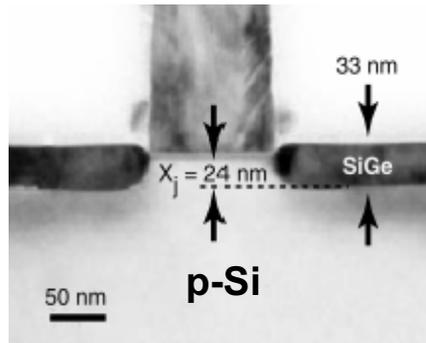
- L = 40 nm and variable contacts (L_C = 20 to 100 nm)
- Smallest contact pitch CP ~ 70 nm, **equivalent to “14 nm” tech. node**

- **Contacts are limiting the performance of small MoS₂ transistors**

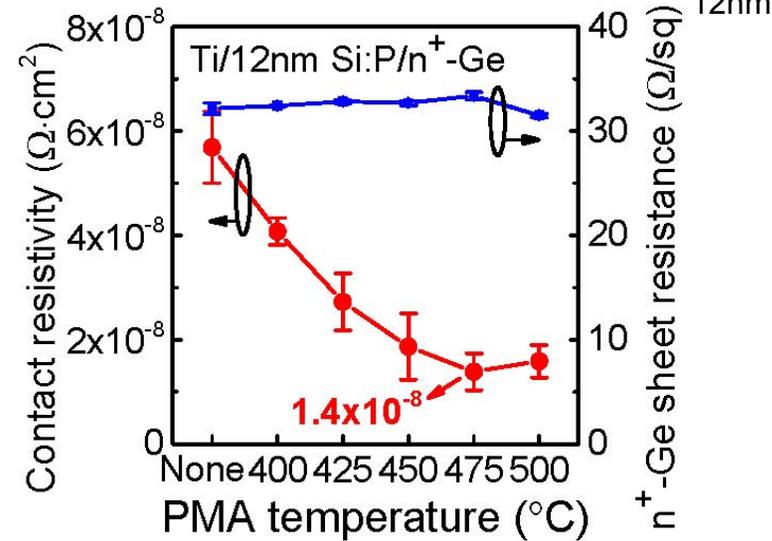
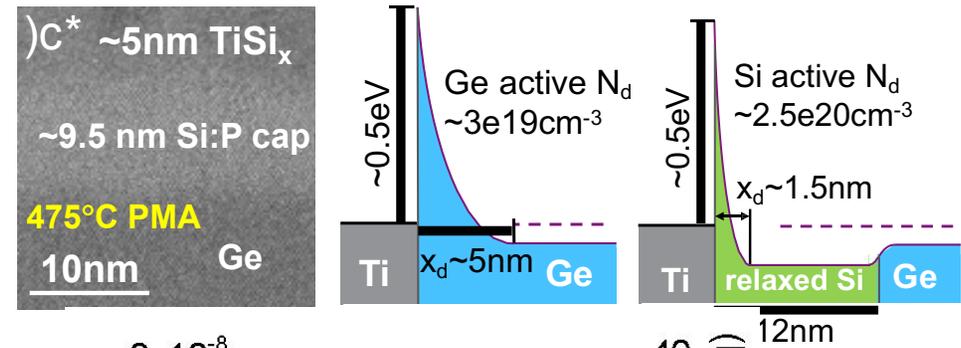
C. English, G. Shine, V. Dorgan, K. Saraswat, E. Pop, *Nano Lett.* 16, 3824 (2016)

Heterostructure Contacts: p-Si and n-Ge

p-SiGe on p-Si



n-Si on n-Ge

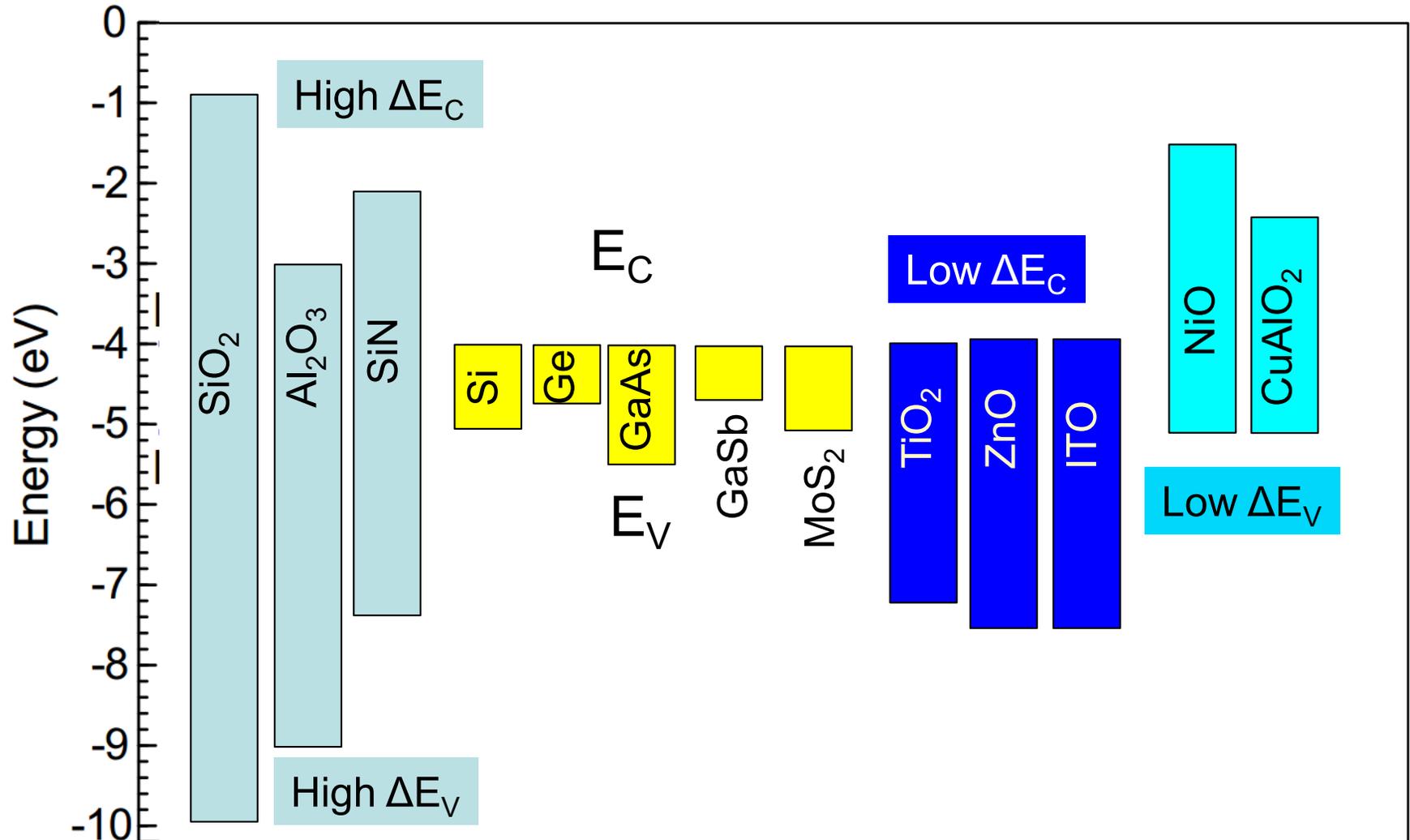


Hao Yu, et al., IEDM 2016

- B activation higher in $\text{Si}_{1-x}\text{Ge}_x$
- lower ϕ_{Bp} > reduction in ρ_c
- Used widely in Si PMOS

- P activation higher in Si than in Ge
- lower ϕ_{Bn} > reduction in ρ_c
- Potential use in Ge NMOS

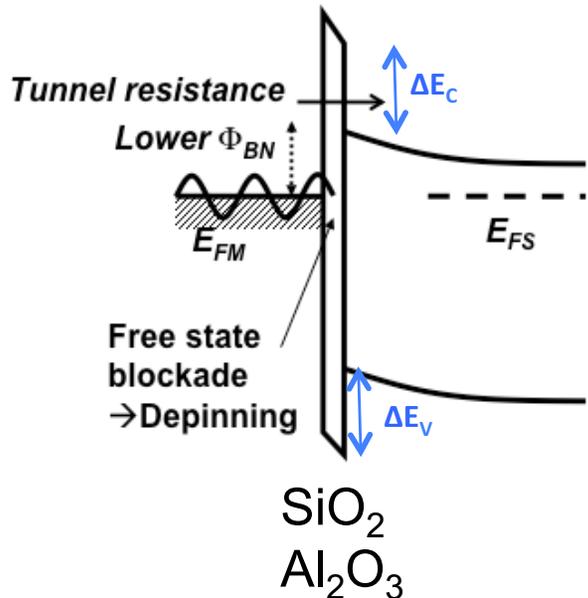
MIS Considerations: Band Alignment



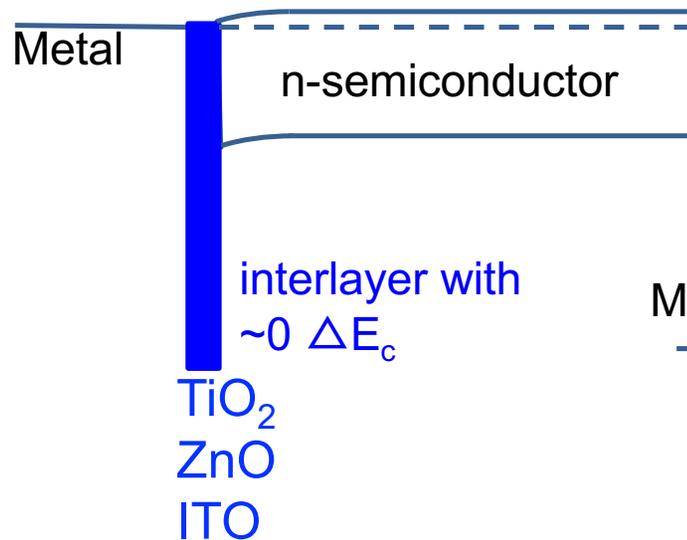
Low band offset needed to minimize tunneling resistance

Ideal MIS Contacts

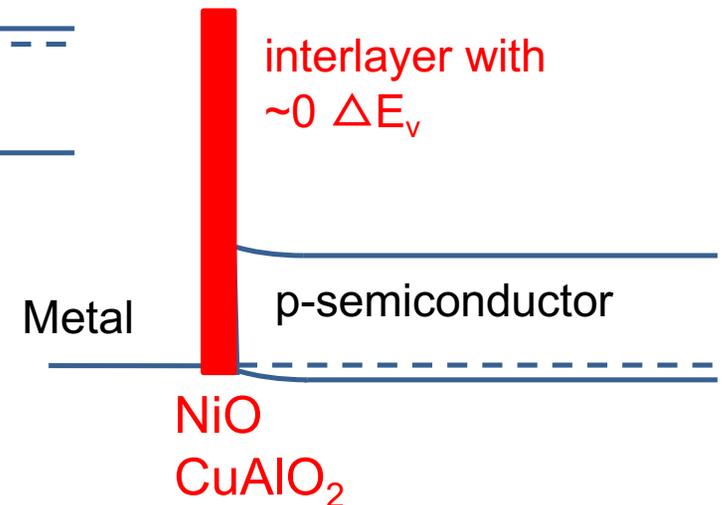
(a) Metal / insulator / semiconductor contact



(b) Metal / $\sim 0 \Delta E_c$ interlayer / n-semiconductor



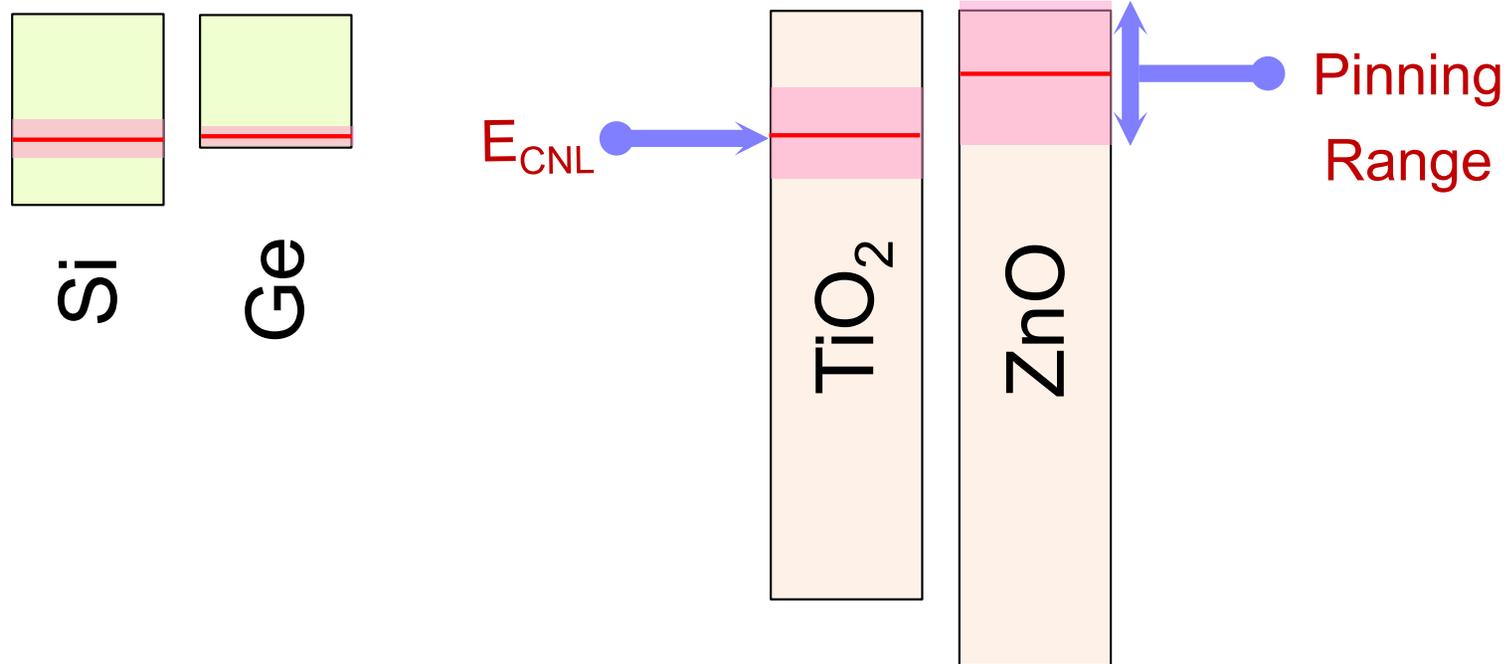
(c) Metal / $\sim 0 \Delta E_v$ interlayer / p-semiconductor



- Large band offset causes tunnel resistance
- Choose interlayer with ~ 0 band offset with semiconductor, pinning factor S closer to 1 and E_{CNL} closer to band edge
- Choose metal with workfunction to align it with the band edges of interlayer and semiconductor

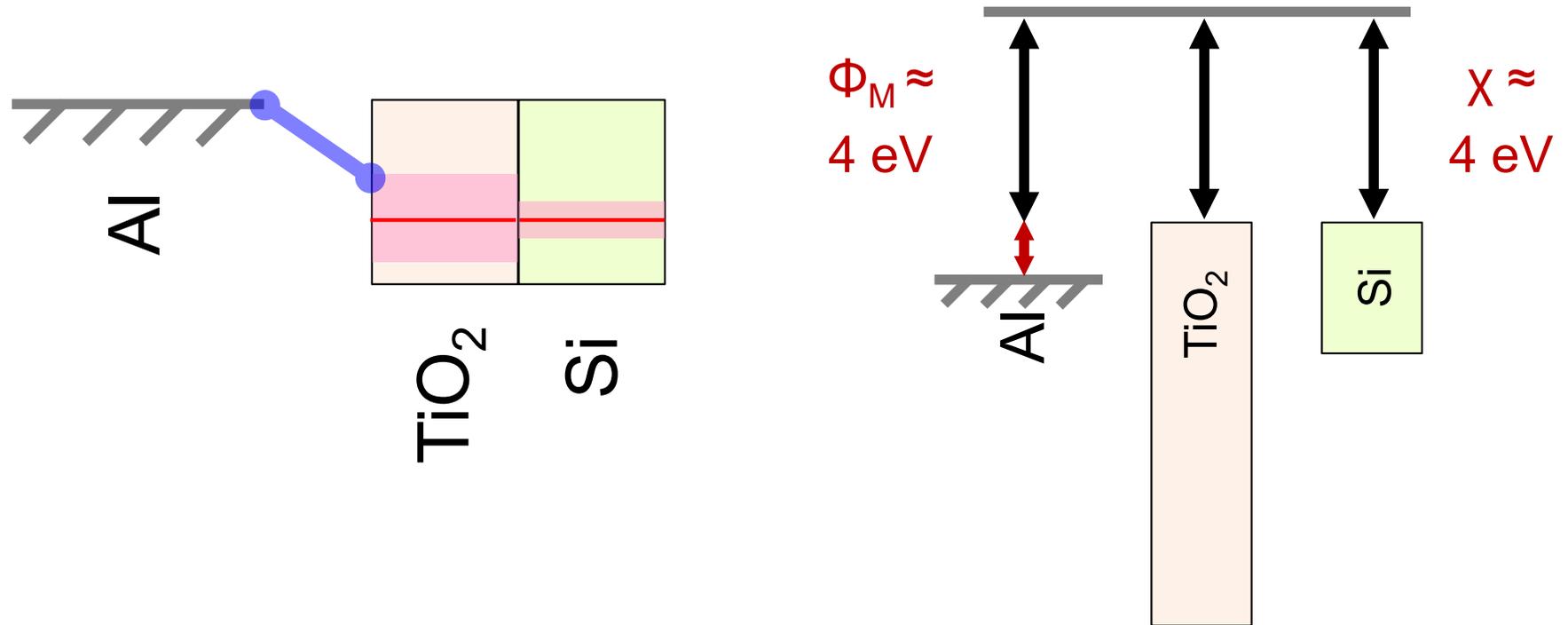
Charge Neutrality Levels

- Band offsets are only part of the story
- ZnO has pinning near the conduction band



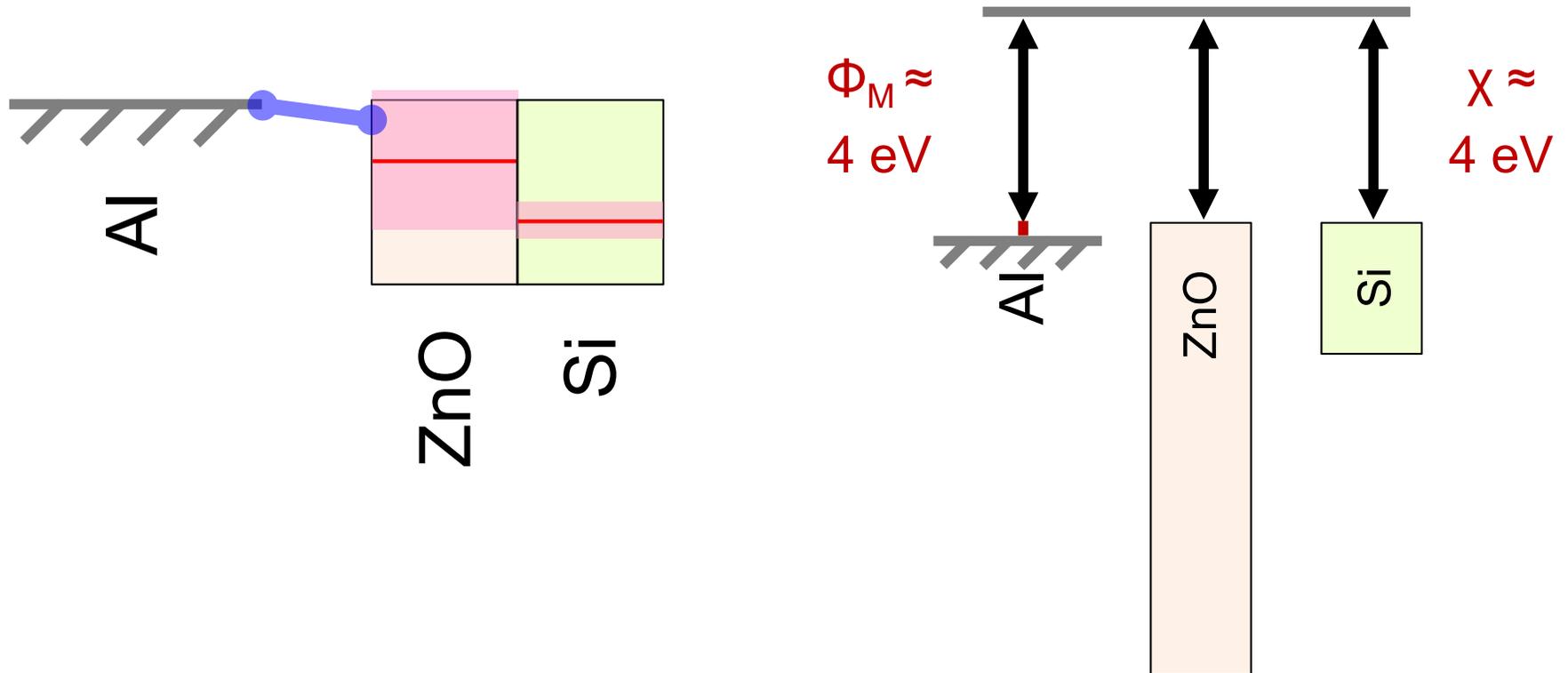
Fermi Level Repinning: TiO₂

- Charge neutrality level is higher up
- More responsive to low metal work functions

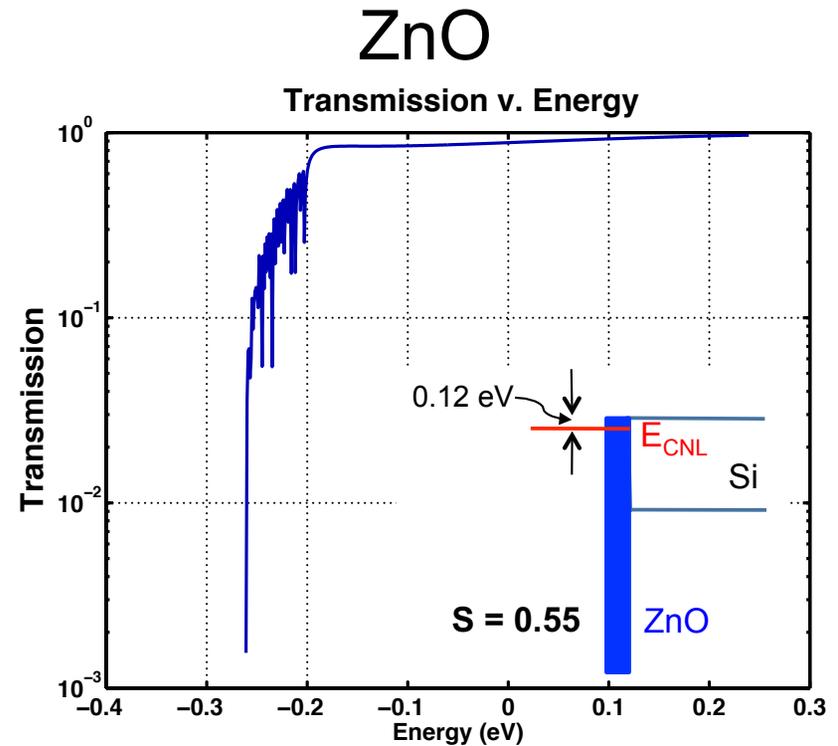
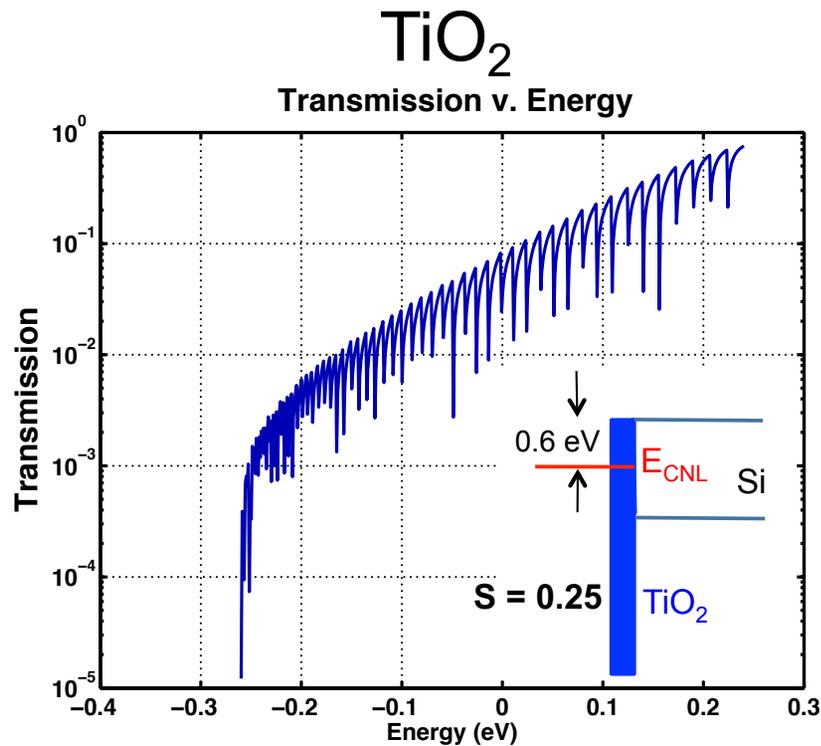


Fermi Level Repinning: ZnO

- Charge neutrality level is higher up
- More responsive to low metal work functions



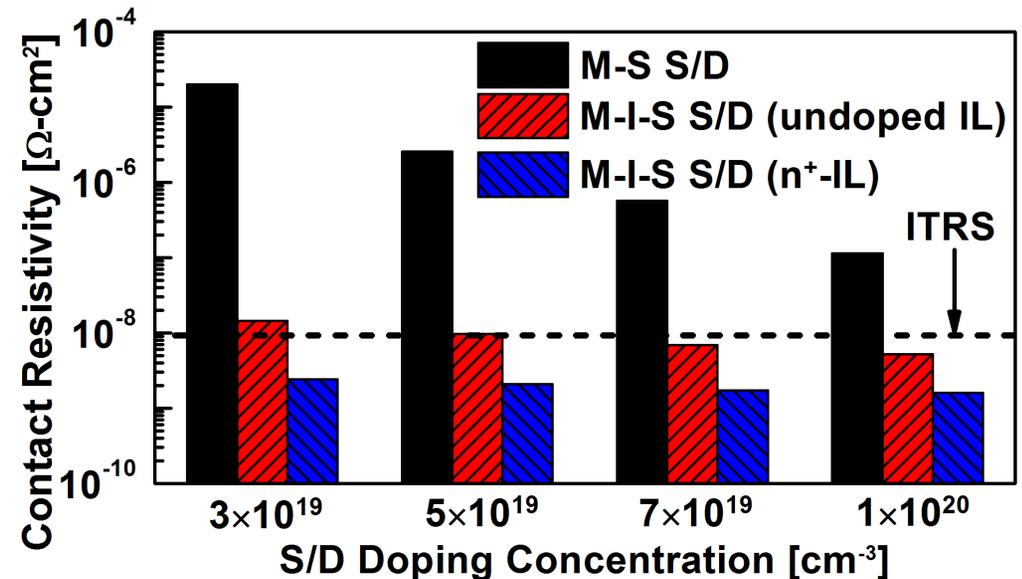
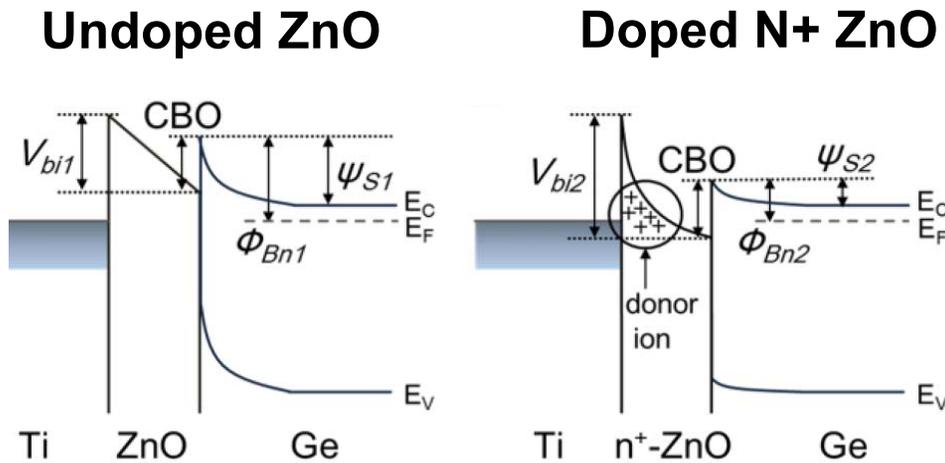
Transmission in MIS Contacts: TiO₂ vs. ZnO



- $10^{-9} \Omega \cdot \text{cm}^2$ requires $T \sim 0.1$ or higher near E_F
- ZnO can achieve this and comes within $\sim 2x$ of the Landauer limit
- ZnO has lower barrier height with metal from better pinning location (E_{CNL} close to conduction band) and is more responsive to metal work function (higher S factor)

Metal/ZnO/n⁺-Ge Contacts: Simulations

ZnO Interlayer $n = 1 \times 10^{21} \text{ cm}^{-3}$



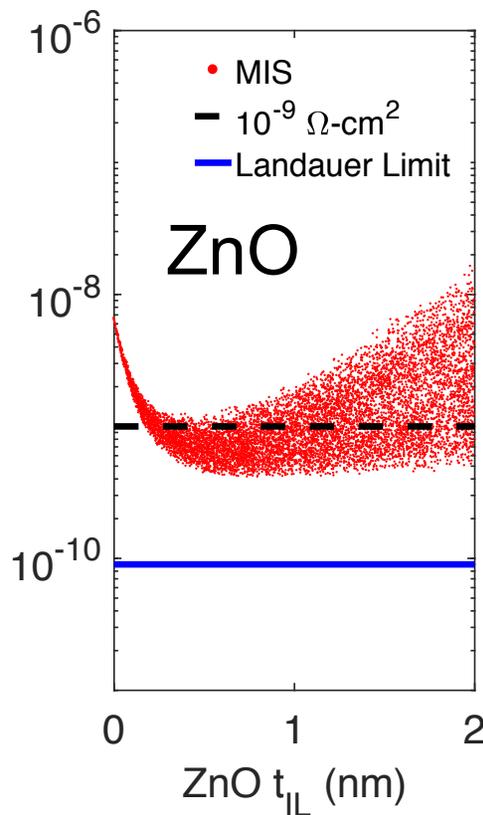
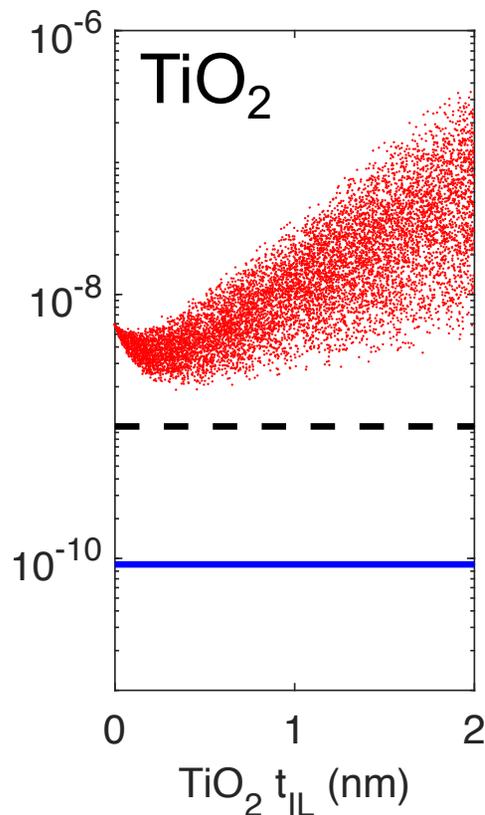
J.-K. Kim,K. Saraswat, H. Y. Yu, IEEE Elec. Dev. Lett. Dec. 2014

- ZnO and ITO can be heavily doped to $n \sim 10^{21} \text{ cm}^{-3} \rightarrow$ low ρ_c
- Ge S/D doping in most of the published work around $1\text{-}3 \times 10^{19} \text{ cm}^{-3}$
- With higher active doping in Ge $\rho_c \sim 2 \times 10^{-9} \text{ } \Omega \cdot \text{cm}^2$ can be achieved

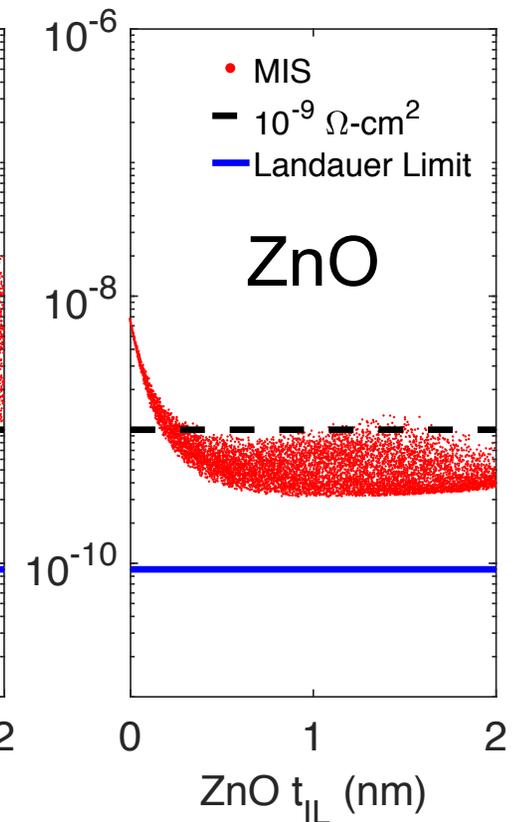
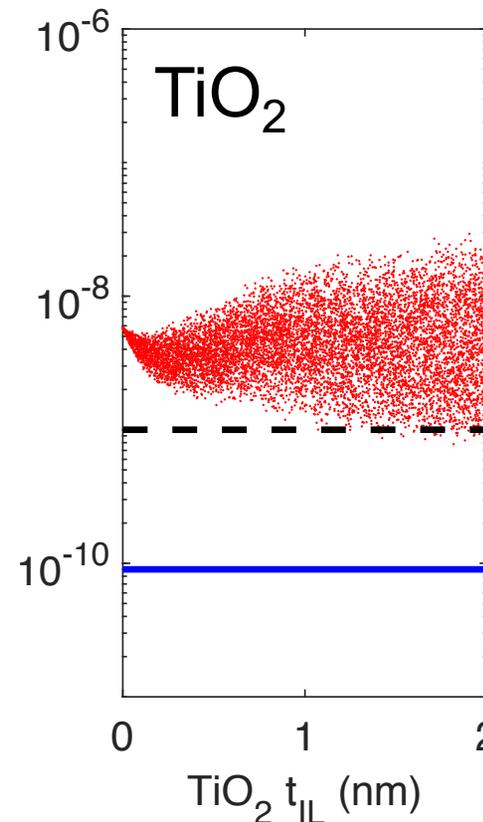
Simulated ρ_c for MIS Contacts to n-Si

Effect of interlayer parameters variation

Interlayer undoped



Interlayer doping of $3 \times 10^{20} \text{ cm}^{-3}$

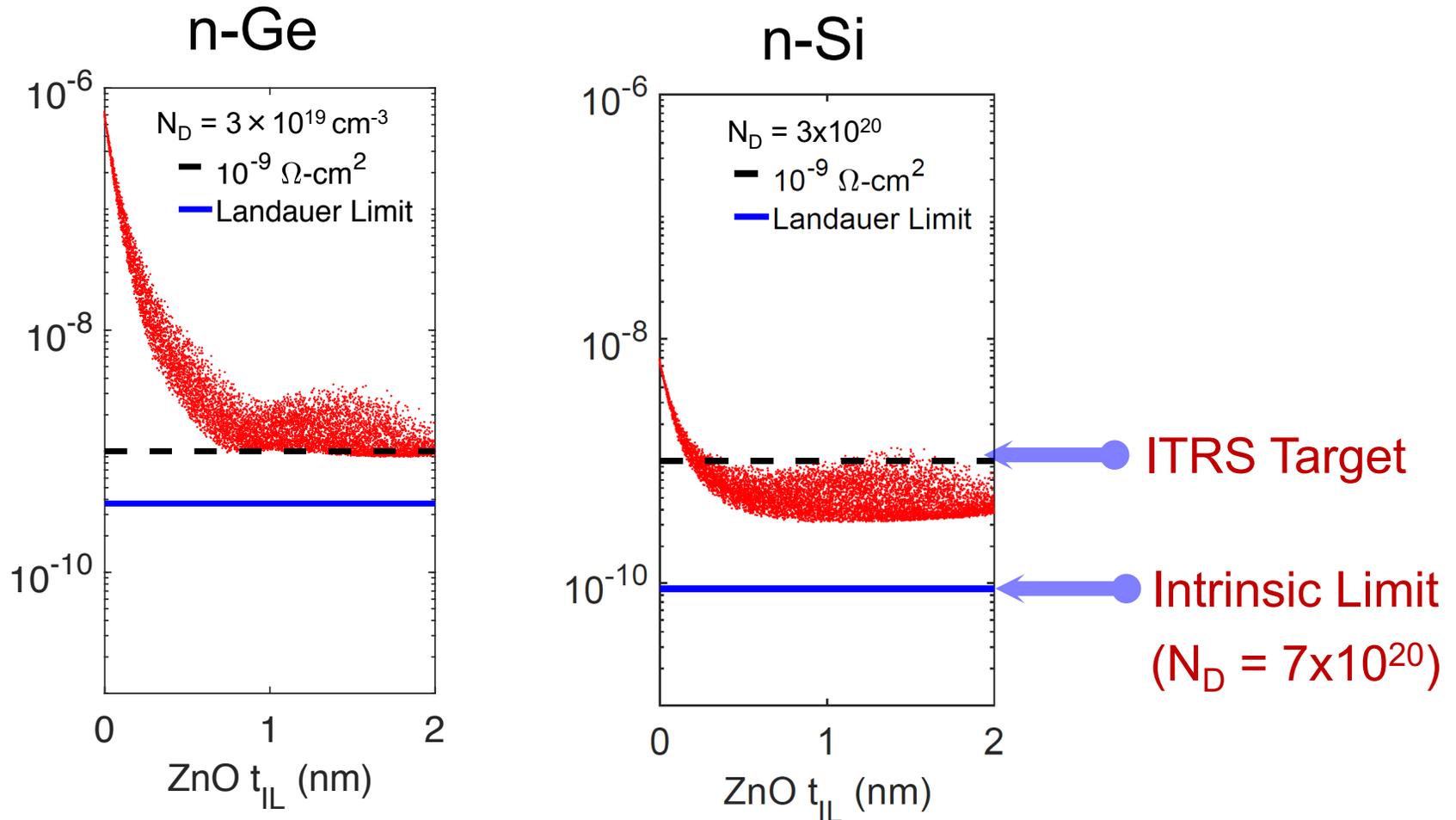


- Silicon $N_D = 3 \times 10^{20} \text{ cm}^{-3}$
- TiO_2 unsuitable for MIS contacts to n-Si
- ZnO is a good candidate to give low ρ_c

G. Shine & K. Saraswat, IEEE TED, Sept. 2017.

Simulated ρ_c for MIS Contacts

Effect of interlayer parameters variation



- ZnO Interlayer doping of $3 \times 10^{20} \text{ cm}^{-3}$
- Even with low Ge doping of $3 \times 10^{19} \text{ cm}^{-3}$ ZnO can give low ρ_c and small variation

Conclusion

- ☹ Contact resistance a major impediment to continued scaling
- 😊 Several methods to reduce contact resistance show promise
 - Heavy doping, heterostructures, depinning Fermi level by MIS
- 😊 For future nodes the materials giving lowest contact resistance may be the choice for MOSFETs.